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**Volari™ XP10
Non-3D Software
Programming Guide**



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1. Overview

This document describes the software programming model for Volari XP10 family products

The Volari XP10 Mobile supports external frame buffer of 32/64/128/256 Mbytes with 64-bit memory bus.

1.1. Key Features

- DX9.0 Vertex Shader 2.0 and Pixel Shader 2.0
- DX9.0c software compatible
- OpenGL 1.5 compatible
- Supports PCI Express for high performance 3D graphics
- 64-bit memory interface Optimized 256-bit 3D graphics engine with Quad-Pixel pipeline
- Digital LCD interface to the internal Dual-Channel LVDS drivers
- Digital LCD interface to both internal and external TMDS drivers
- Advanced De-Interlacing algorithm for displaying standard interlaced video on progressive VGA monitor.
- Hardware support of DVD video playback with Motion Compensation and Inverse Discrete Cosine Transform
- Integrated 420MHz RAMDAC™ and clock synthesizer
- Resolutions up to 2048x1536
- Linear addressing up to 4GB memory space
- Supports VESA™ Display Data Channel (DDC) & DPMS protocol
- Memory mapped I/O and instruction FIFOs for graphics engine operations
- Re-locatable memory mapped I/O for all registers in PCIe configuration
- Fully compliant IBM® VGA and VESA™ extended VGA modes
- Embedded TV-Out feature (built-in TVX2)

1.2. This Manual

The purpose of this *Software Programmer's Guide* (SPG) is to document the use of the internal registers and BIOS functions. Some implementation examples are included. Additional information can be obtained in the Volari XP10 *Technical Reference Manual* (TRM).



1.3. Register Summary

The Volari XP10 features the following register sets, which are grouped into functional categories:

- Standard VGA Register Set: General Registers, Sequencer Registers, CRT Controller Registers, Graphics Controller Registers, Attribute Controller Registers, and Setup Registers.
- Extended Mode Register Set: registers specific to advanced features of the Volari XP10. Examples of Extended Registers are: the DRAM Clock Select Register, Performance Tuning Register, and Read Cache Control Register
- Memory Interface Register Set: registers for control DDR SDRAM memory.
- Hardware Cursor Register Set: registers for controlling Hardware Cursor position, pattern location, and offset.
- SYNDAC Frequency Synthesizer Register Set: registers for controlling the internal DAC and memory clock timing parameters.
- Video Display and Capture Engine Register Set: registers for controlling dual video window displays, video and graphics overlay, capture, and the Hi-Fi video processor.
- New Video Display Register Set
- PCIE Interface Register Set: registers to set the PCIExpress configuration space.
- Interrupt and Bus Mastering Register Set: registers for the response of interrupt sources and registers for PCI Bus Master programming.
- Power Management Register Set: registers for the DPMS program for the Volari XP10.
- Flat Panel Control Registers: registers to control flat panels Volari XP10.
- CRTC Shadow Registers Set: registers to control CRTC Shadow.
- 3D Graphics Engine Register Set: registers for 3D image and graphics processing; including: drawing environment setup and frame buffer control, drawing command, geometry engine setup, and primitive setup with sequential loading.
- Digital TV Encoder Interface Register Set: registers for controlling the Digital Encoder interface.
- DVD Video Register Description



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2. BIOS Specifications

This section describes the BIOS specifications for the XP10 series GPU. The BIOS supports all VGA modes, and VESA™ BIOS extension modes.

2.1. Functional Features

The following is a list of the BIOS functional features:

- Compatible with IBM® VGA BIOS through Int.10H Function calls as listed in this document.
- Support of VESA™ BIOS Extension (VBE) 2.0. The entire VBE is in the BIOS, requiring no help from any memory resident programs.
- 48K Bytes of BIOS size for easy motherboard applications that include all the modes listed in this specification.
- Enhanced Display Data Channel communication support for DDC2B between the computer display and the host system.
- PCI jumper-less sleep mode support.
- Compatible with VESA™ mode specifications.
- Variable refresh rates as listed in this document.
- Provides built-in TV-out (TVX2) and Digital Video Interface (DVI) output.
- Supports up to 16 different LCD panels (XP10).
- Supports dual display modes, which consist of combinations of LCD-CRT and LCD-TV.
- Supports triple display modes. The Volari XP10 supports three simultaneous displays that would consist of LCD or DVI, CRT, and TV all actively displaying images at the same time.
- Enhanced XGI functions such as Extended Setmode and Display Device Switching.

Note: All features may not be implemented simultaneously due to BIOS space limitations.

2.2. Graphics Mode Support

The Volari XP10 BIOS supports all VGA, EGA, and monochrome modes, and it supports high-resolution modes with a variety of refresh rates. The Volari XP10 BIOS will make these modes available by first checking that there is sufficient memory and that the memory clock is fast enough to support the mode.

The BIOS mode tables shown below are carefully configured to support DDC2B applications by taking full advantage of features of the Volari XP10 Accelerator. The BIOS modes are IBM® VGA BIOS compatible.



2.2.1. Standard Modes

Table 2-1 Standard Modes

Mode	Type	Color	Alpha Format	Cell Size	Screen Format
0, 1	Text	16	40x25	8x8	320x200
0*, 1*	Text	16	40x25	8x14	320x350
0+, 1+	Text	16	40x25	9x16	360x400
2,3	Text	16	80x25	8x8	720x200
2*, 3*	Text	16	80x25	8x14	640x350
2+, 3+	Text	16	80x25	9x16	720x400
4,5	Graphics	4	40x25	8x8	320x200
6	Graphics	4	80x25	8x8	640x200
7	Text	4	80x25	9x14	720x350
7+	Text	4	80x25	9x16	720x400
D	Graphics	16	40x25	8x8	320x200
E	Graphics	16	80x25	8x8	640x200
F	Graphics	4	80x25	8x14	640x350
10	Graphics	16	80x25	8x14	640x350
11	Graphics	2	80x30	8x16	640x480
12	Graphics	16	80x30	8x16	640x480
13	Graphics	256	40x25	8x8	320x200

2.2.2. Extended Modes

Table 2-2 Extended Text Modes

Mode	Type	Color (bits)	Alpha Format	Cell Size	Screen Format	Refresh Rate (Hz)
50	Text	16	80x30	8x16	640x480	60
51	Text	16	80x43	8x11	640x473	60
52	Text	16	80x60	8x8	640x480	60
53	Text	16	132x25	8x14	1056x350	70
54	Text	16	132x30	8x16	1056x480	60
55	Text	16	132x43	8x11	1056x473	60
56	Text	16	132x60	8x8	1056x480	60



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57	Text	16	132x25	9x14	1188x350	70
58	Text	16	132x30	9x16	1188x480	60
59	Text	16	132x43	9x11	1188x473	60
5A	Text	16	132x60	9x8	1188x480	60

Table 2-3 Extended Graphics Modes

Mode	Type	Color (bits)	Screen Format	Refresh Rate (Hz)
30	Graphics	8,15,16,32	320x200	70
31	Graphics	8,15,16,32	320x240	60/75/85
32	Graphics	8,15,16,32	400x300	60/75/85
33	Graphics	8,15,16,32	512x384	87i/60/75/85
38	Graphics	8,15,16,32	720x480	60
3A	Graphics	8,15,16,32	720x576	60
5B	Graphics	4	800x600	60/75/85
5C	Graphics	4	1024x768	87i/60/75/85
5D	Graphics	4	1280x1024	87i/60/75/85
5E	Graphics	4	1600x1200	96i/60
60	Graphics	8,15,16,32	640x400	70/85
61	Graphics	8,15,16,32	640x480	60/75/85/100/120
62	Graphics	8,15,16,32	800x600	60/75/85/100/120
63	Graphics	8,15,16,32	1024x768	87i/60/75/85/100/120
64	Graphics	8,15,16,32	1280x1024	87i/60/75/85/100
65	Graphics	8,15,16,32	1600x1200	96i/60/75/85
66	Graphics	8,15,16,32	1920x1440	60
67	Graphics	8,15,16,32	2048x1536	60
68	Graphics	8,15,16,32	1152x864	60/75/85

2.3. VESA™ Support

The Volari XP10 supports VESA™ standards, including VBE, VESA™ DDC, and VESA™ DPMS standards.

2.3.1. VESA™ BIOS Extensions (VBE)

The Volari XP10 is compliant with VBE 2.0. VBE 2.0 provides a common software interface for Super VGA graphics products. It enables application and system software to adapt to and utilize the wide range of features available in the Volari XP10. The VBE 2.0 function calls that follow are available.



2.3.1.1. VBE 2.0 Function 00h—Return VBE Controller Information

This function returns the capabilities of the display controller, the revision level of the VBE implementation, and vendor specific information to assist in supporting all display controllers in the field.

The purpose of this function is to provide information to the calling program about the general capabilities of the installed VBE software and hardware. This function fills an information block structure at the address specified by the caller. The VbeInfoBlock information block size is 256 bytes for VBE 1.x, and 512 bytes for VBE 2.0.

Function	Register	Description
Entry	AX	4F00h (Return VBE Controller information)
	ES:DI	Pointer to buffer in which to place VbeInfoBlock structure
Return	AX=	VBE Return Status

Note: All other registers are preserved. For more information on the Controller Information Block see VBE 2.0 specifications.

2.3.1.2. VBE 2.0 Function 01h—Return VBE Mode Information

This function returns extended information about a specific VBE display mode from the mode list returned by VBE Function 00h. This function fills the mode information block, ModeInfoBlock, structure with technical details on the requested mode. The ModeInfoBlock structure is provided by the application with a fixed size of 256 bytes.

Information can be obtained for all listed modes in the VideoModeList returned in Function 00h. If the requested mode cannot be used or is unavailable, a bit will be set in the ModeAttributes field to indicate that the mode is not supported in the current configuration.

Function	Register	Description
Entry	AX=	4F01h (Return VBE mode information)
	CX=	Mode number
	ES:DI	Pointer to ModeInfoBlock structure
Return	AX=	VBE Return Status

Note: All other registers are preserved. For more information on the Mode Information Block see VBE 2.0 specifications.

2.3.1.3. VBE 2.0 Function 02h—Set VBE Model

This function initializes the controller and sets a VBE mode. The format of VESA VBE mode numbers is described earlier in this document. If the mode cannot be set, the BIOS should leave the graphics environment unchanged and return a failure error code.



Function	Register	Description
Entry	AX=	4F02h (Set VBE Mode)
	BX=	Desired Mode to set D0 - D13 = Mode number D14 = 0 : Linear address disabled 1 : Linear address enabled D15 = 0 : Clear display memory 1 : Don't clear display memory
Return	AX=	VBE Return Status

Note: All other registers are preserved. For more information on Set VBE Mode see VBE 2.0 specifications.

2.3.1.4. VBE 2.0 Function 03h—Return Current VBE Mode

This function returns the current VBE mode. The format of VBE mode numbers is described earlier in this document:

Function	Register	Description
Entry	AX=	4F03h (Return Current VBE Mode)
Return	AX=	VBE Return Status

Note: All other registers are preserved. For more information on Current VBE Mode see VBE 2.0 specifications.



2.3.1.5. VBE 2.0 Function 04h—Save/Restore State

This required function provides a complete mechanism to save and restore the display controller hardware state. The functions are a superset of the three Sub-functions under the standard VGA BIOS Function 1Ch (Save/restore state), which does not guarantee that the extended registers of the video device are saved or restored. The complete hardware state (except frame buffer memory) should be saveable/restorable by setting the requested states mask (in the CX register) to 000Fh.

Function	Register	Description
Entry	AX=	4F04h (Save/Restore State)
	DL=	00h Return Save/Restore State buffer size 01h Save Super VGA state 02h Restore Super VGA state
	CX=	Requested States
		D0 Save/Restore controller hardware state D1 Save/Restore BIOS data state D2 Save/Restore DAC state D3 Save/Restore Super VGA state
	ES:BX	Pointer to buffer (if DL <> 00h)
Return	AX=	VBE Return Status
	BX=	Number of 64-byte blocks to hold the state buffer (if DL=00h)

Note: All other registers are preserved. For more information on Save/Restore State see VBE 2.0 specifications.



2.3.1.6. VBE 2.0 Function 05h—Display Window Control

This function sets or gets the position of the specified display window or page in the frame buffer memory by adjusting the necessary hardware paging registers. To use this function properly, the software should first use VBE Function 01h (Return VBE Mode information) to determine the size, location and granularity of the windows.

For performance reasons, it may be more efficient to call this function directly, without incurring the INT 10h overhead. VBE Function 01h returns the segment: offset of this windowing function that may be called directly for this reason. Note that a different entry point may be returned based upon the selected mode. Therefore, it is necessary to retrieve this segment: offset specifically for each desired mode.

Function	Register	Description
Entry	AX=	4F05h (VBE Display Window Control)
	BH=	00h : Select memory window 01h : Return memory window
	BL=	Window Number: 00h=Window A 01h=Window B
	DX=	Window number in video memory in window granularity units(Set Memory Window only)
Return	AX=	VBE Return Status
	DX=	Window number in window granularity units (Get Memory Window only)

Note: For more information on Display Window Control see VBE 2.0 specifications.

2.3.1.7. VBE 2.0 Function 06h—Set/Get Logical Scan Line Length

This function sets or gets the length of a logical scan line. This allows an application to set up a logical display memory buffer that is wider than the displayed area. VBE Function 07h (Set/Get Display Start) then allows the application to set the starting position that is to be displayed.

Function	Register	Description
Entry	AX=	4F06h VBE Set/Get Logical Scan Line Length
	BL=	00h (Set Scan Line Length) 01h (Get Scan Line Length)
	CX=	If BL=00h Desired Width in Pixels If BL=02h Desired Width in Bytes
Return	AX=	VBE Return Status
	BX=	Bytes Per Scan Line
	CX=	Actual Pixels Per Scan Line (truncated to nearest completed pixel)



	DX=	Maximum Number of Scan Lines
--	-----	------------------------------

Note: For more information on Set/Get Logical Scan Line Length see VBE 2.0 specifications.

2.3.1.8. VBE 2.0 Function 07h—Set/Get Display Start

This function selects the pixel to be displayed in the upper left corner of the display. This function can be used to pan and scroll around logical screens that are larger than the displayed screen. This function can also be used to rapidly switch between two different displayed screens for double-buffered animation effects.

Function	Register	Description
Entry	AX	4F07h (VBE Set/Get Display Start Control)
	BH	00h (Reserved and must be 00h)
	BL	00h (Set Display Start) 01h (Get Display Start)
	CX	First Display Pixel In Scan Line (Set Display Start only)
	DX	First Display Scan Line (Set Display Start only)
Return	AX	VBE Return Status
	BH	00h Reserved and will be 0 (Get Display Start only)
	CX	First Displayed Pixel In Scan Line (Get Display Start only)
	DX	First Displayed Scan Line (Get Display Start only)

Note: For more information on Set/Get Display Start Control see VBE 2.0 specification. VESA did not define whether the first point is (0,0) or (1,1), so we assume it's (0,0).

2.3.1.9. VBE 2.0 Function 08h—Set/Get DAC Palette Format

This function manipulates the operating mode or format of the DAC palette. Some DACs are configurable to provide 6 bits, 8 bits, or more of color definition per red, green, and blue primary colors. The DAC palette width is assumed to be reset to the standard VGA value of 6 bits per primary color during any mode set.

Function	Register	Description
Entry	AX=	4F08h (VBE Set/Get Palette Format)
	BL=	00h (Set DAC Palette Format) 01h Get DAC Palette Format
	BH=	Desired bits of color per primary (Set DAC Palette Format only)
Return	AX	VBE Return Status
	BH	Current number of bits of color per primary

Note: For more information on Set/Get Palette Format see VBE 2.0 specifications.



2.3.1.10. VBE 2.0 Function 09h—Set/Get Palette Data

This function is very important for RAMDAC™'s that are larger than a standard VGA RAMDAC™. The standard INT 10h BIOS Palette function calls assume standard VGA ports and VGA palette widths. This function offers a palette interface that is independent of the VGA assumptions.

Function	Register	Description
Entry	AX=	4F09h (VBE 2.0 Set/Get Palette Data)
	BL=	00h Set Palette Data 01h Get Palette Data 02h Set Secondary Palette Data 03hGet Secondary Palette Data 80h Set Palette Data during Vertical Retrace with Blank Bit on
	CX	Number of palette registers to update (to a maximum of 256)
	DX	First of the palette register to update (start)
	ES:DI	Table of palette values (see below for format)
Return	AX	VBE Return Status

Note: For more information on Set/Get Palette Data see VBE 2.0 specifications.

2.3.1.11. VBE 2.0 Function 0Ah—Return VBE Protected Mode Interface

This function call returns a pointer to a table that contains code for a 32-bit protected mode interface that can either be copied into local 32-bit memory space or can be executed from ROM providing the calling application sets all required selectors and I/O access correctly. This function returns a pointer (in real mode space) with offsets to the code fragments, and additionally returns an offset to a table which contains Non-VGA Port and Memory locations which an Application may have to have I/O access to.

Function	Register	Description
Entry	AX=	0Ah (VBE 2.0 Protected Mode Interface)
	BL=	Return protected mode table
Return	AX	Status
	ES	Real Mode Segment of Table
	DI	Offset of Table
	CX	Length of Table including protected mode code in bytes (for copying purposes)

Note: For more information on Protected Mode Interface see VBE 2.0 specifications.

**2.3.1.12. VBE 2.0 Function 10h—Power Management**

The following function queries and selects the power management-operating mode. The following tables display the register settings for the function call:

Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	10h (VBE/PM Services)
	BL=	00h (Report VBE/PM Capabilities)
	CX=	00h (Primary Display) (See note below)*
Return	AX=	Status
	BH =	Power saving state signals supported by the controller: 1 = supported; 0 = not supported. 00h ON 01h STANDBY 02h SUSPEND 04h OFF
	BL=	VBE/PM version number (0001000 for this version)
	CX=	Unchanged

Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	10h (VBE/PM Services)
	BL=	01h (Set Display Power State)
	BH=	Requested power states: 00h ON 01h STANDBY 02h SUSPEND 04h OFF
	CX=	00h (Primary Display) (See note below)*
Return	AX=	Status
	BH=	Unchanged
	CX=	Unchanged



Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	10h (VBE/PM Services)
	BL=	02h (Get Display Power State)
	CX=	See note below *
Return	AX=	Status
	BH=	Power states currently requested by the controller: 00h ON 01h STANDBY 02h SUSPEND 04h OFF

* For multi-display devices, this function can be extended as below:

BL= 81h	Set display power state
82h	Get display power state
CX= 00h	VESA compatible (all displays)
D0h	LCD (on/off only)
D1h	CRT
D2h	TV (Reserved)
D3h	DVI

2.3.1.13. VBE 2.0 Function 11h—Get Flat Panel Information

The following tables display the register settings for the function call:

Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	11h (VBE/FP Services)
	BL=	01h (Return flat panel information)
	ES:DI=	Pointer to a 32-byte buffer
Return	AX=	Status



2.3.2. VESA™ DDC2B

2.3.2.1. DDC2B Interface Protocol

The DDC2B VGA Subsystem BIOS will make an Extended Display Identification (EDID) request to the display unit. If there is no response from the display or if repeated errors are detected, the VGA Subsystem BIOS shall assume that the display is a type “Old” and shall resume as type “Old” monitor.

2.3.2.2. DDC2B S/W Progress During and After POST

During the POST the VGA Subsystem BIOS pulls the SCL line low indicating that it has DDC2B support. The VGA Subsystem BIOS can then obtain EDID data from the monitor at the request of the System BIOS. During that time, the System BIOS will allocate 128 Bytes of System Memory for temporary use to the VGA Subsystem BIOS.

2.3.2.3. VBE Sub-function Call 15h for Display Identification Extensions

The following function queries and selects the operating mode of the display identification extensions. The following tables display the register settings for this function call:

Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	15h (VBE/DDC Services)
	BL=	00h (Report VBE/PM Capabilities)
	CX=	00h (Controller unit number)
	ES:DI=	Null
Return	AX=	Status
	BH =	Approx.
	BL=	DDC level supported.

2.3.2.4. VBE Function 15h—Read EDID

The following function queries and selects the operating mode of Read EDID. The following tables display the register settings for this function call:

Function	Register	Description
Entry	AH=	4Fh (VESA™ Extension)
	AL=	15h (VBE/DDC Services)
	BL=	01h (Read EDID)
	CX=	00h (Controller unit number) (See note below)*



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	DX=	00h (EDID block number)
	ES:DI=	Pointer to area in which the EDID block is returned.
Return	AX=	Status
	ES:DI =	Pointer to area in which the EDID block is returned.

* For multi-display devices, this function can be extended as below:

CX=00h	VESA compatible (CRT display) Get EDID from active display either CRT or DVI. If both displays are active, it will get the EDID of display that has lower capability.
D0h	LCD (Reserved)
D1h	CRT
D2h	TV (Reserved)
D3h	DVI

If the above call is successful, the following data can be found at location ES:DI as specified by the caller of the function.

No. of Bytes	Description
8	Header
10	Vendor/Product Identification
2	EDID Version/Revision
15	Basic Display Parameters
19	Established/Standard Timing
72	Detailed timing description (18 bytes each)
1	Extension Flag
1	Checksum



2.3.3. VESA™ CRTC Timing

2.3.3.1. Vertical Timing

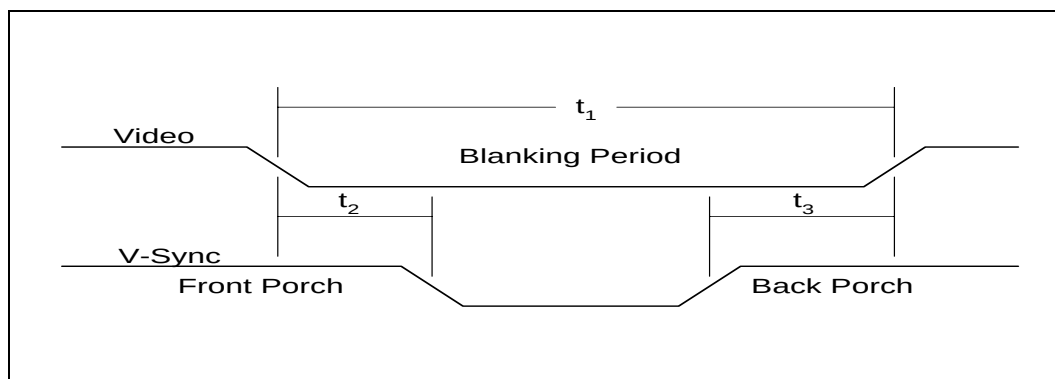


Table 2-4 Vertical Timing

Display	Refresh Rate (HZ)	Blanking Period T1 (MS)	Front Porch T2 (MS)	Back Porch T3 (MS)	Polarity
640x480	60	0.922	0.064	0.794	Negative
640x480	75	0.533	0.027	0.427	Negative
640x480	85	0.670	0.023	0.578	Negative
640x480	100	N/A	N/A	N/A	Negative
640x480	120	N/A	N/A	N/A	Negative
800x600	60	0.739	0.026	0.607	Positive
800x600	75	0.533	0.021	0.448	Positive
800x600	85	0.578	0.019	0.503	Positive
800x600	100	N/A	N/A	N/A	Positive
800x600	120	N/A	N/A	N/A	Positive
1024x768	87i	1.351	0.000	1.126	Positive
1024x768	60	0.786	0.062	0.600	Negative
1024x768	75	0.533	0.017	0.466	Positive
1024x768	85	0.582	0.015	0.524	Positive
1024x768	100	N/A	N/A	N/A	Positive
1024x768	120	N/A	N/A	N/A	Positive
1280x1024	87i	0.948	0.043	0.775	Positive



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Display	Refresh Rate (HZ)	Blanking Period T1 (MS)	Front Porch T2 (MS)	Back Porch T3 (MS)	Polarity
1280x1024	60	0.656	0.016	0.594	Positive
1280x1024	75	0.526	0.013	0.475	Positive
1280x1024	85	0.527	0.011	0.483	Positive
1280x1024	100	N/A	N/A	N/A	Positive
1600x1200	96i	1.600	0.032	1.472	Positive
1600x1200	60	0.667	0.013	0.613	Positive
1600x1200	75	N/A	N/A	N/A	Positive
1600x1200	85	N/A	N/A	N/A	Positive
1600x1200	100	N/A	N/A	N/A	Positive
1920x1440	60	N/A	N/A	N/A	Positive
1920x1440	75	N/A	N/A	N/A	Positive
2048x1536	60	N/A	N/A	N/A	Positive
2048x1536	75	N/A	N/A	N/A	Positive

2.3.3.2. Horizontal Timing

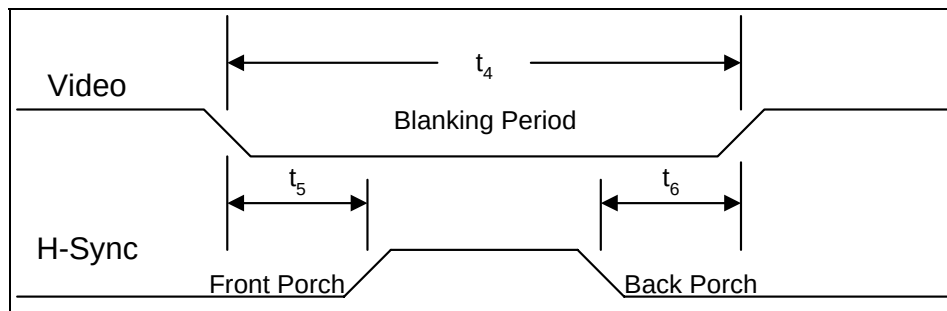


Table 2-5 Horizontal Timing

Display	Refresh Rate (HZ)	Blanking Period T4 (μ S)	Front Porch T5 (μ S)	Back Porch T6 (μ S)	Polarity
640x480	60	5.720	0.318	1.589	Negative
640x480	75	6.349	0.508	3.810	Negative
640x480	85	5.333	1.556	2.222	Negative
640x480	100	N/A	N/A	N/A	Negative



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Display	Refresh Rate (HZ)	Blanking Period T4 (μS)	Front Porch T5 (μS)	Back Porch T6 (μS)	Polarity
640x480	120	N/A	N/A	N/A	Negative
800x600	60	6.400	1.000	2.200	Positive
800x600	75	5.172	0.323	3.232	Positive
800x600	85	4.409	0.569	2.702	Positive
800x600	100	N/A	N/A	N/A	Positive
800x600	120	N/A	N/A	N/A	Positive
1024x768	87i	5.345	0.0178	1.247	Positive
1024x768	60	4.923	0.369	2.462	Negative
1024x768	75	3.657	0.203	2.235	Positive
1024x768	85	3.725	0.508	2.201	Positive
1024x768	100	N/A	N/A	N/A	Positive
1024x768	120	N/A	N/A	N/A	Positive
1280x1024	87i	5.283	0.203	4.063	Positive
1280x1024	60	3.778	0.148	2.593	Positive
1280x1024	75	3.007	0.119	1.837	Positive
1280x1024	85	N/A	N/A	N/A	Positive
1280x1024	100	N/A	N/A	N/A	Positive
1600x1200	96i	4.148	0.237	2.489	Positive
1600x1200	60	2.440	0.279	1.325	Positive
1600x1200	75	N/A	N/A	N/A	Positive
1600x1200	85	N/A	N/A	N/A	Positive
1600x1200	100	N/A	N/A	N/A	Positive
1920x1440	60	N/A	N/A	N/A	Positive
1920x1440	75	N/A	N/A	N/A	Positive
2048x1536	60	N/A	N/A	N/A	Positive
2048x1536	75	N/A	N/A	N/A	Positive

2.3.4. PCI Support

2.3.4.1. PCI Configuration for Volari XP10

The Device ID, Vendor ID and Class code information required for the Volari XP10 can be found in the standard PCI Configuration space in their respective locations as defined in the PCI Local Bus specification published by the PCI



SIG. For ease of reference, the following table displays the specific identification data for the Volari XP10:

PCI Config Space	Description	Data
Byte 01h and 00h	Vendor ID	18CA
Byte 03h and 02h	Device ID	0047

2.3.5. BIOS Power On Sequence

The Volari XP10 can be programmed by the following sequence:

1. Enable VGA chip by 3C3h.
2. Configure memory interface.
3. Configure panel by INT 15h (or by external configuration).
4. Relocate panel information.
5. Update the checksum.
6. Program extended registers.
7. Configure TV system.
8. Configure default display device by INT 15h (or by external configuration).
9. Initialize memory and detect attached memory.
10. Standard VGA POST.

2.3.6. Int 10h Calls

2.3.6.1. Standard Int 10h Functions

The Interrupt 10H calls provide a variety of functions in addition to the VBE function calls. This manual provides detailed programming examples and explanations. The table on the following pages summarizes all of the function calls available for the Volari XP10

Table 2-6 Standard INT 10H Function Summary

Function	Sub-function	Description	Adapter
00H		Set video mode.	EGA, VGA
01H		Set cursor type.	EGA, VGA
02H		Move cursor.	EGA, VGA
03H		Get cursor location/type.	EGA, VGA
04H		Reserved.	EGA, VGA
05H		Select active page.	EGA, VGA



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Function	Sub-function	Description	Adapter
06H		Scroll window up.	EGA, VGA
07H		Scroll window down.	EGA, VGA
08H		Read character/attribute at current cursor position.	EGA, VGA
09H		Write character/attribute to current cursor position.	EGA, VGA
0AH		Write characters to current cursor position.	EGA, VGA
0BH	00H	Set color palette.	EGA, VGA
0CH		Write dot.	EGA, VGA
0DH		Read dot.	EGA, VGA
0EH		Write TTY to active page.	EGA, VGA
0FH		Read video state.	EGA, VGA
10H		Set palette registers.	EGA, VGA
	00H	Set individual palette register.	
	01H	Set overscan register.	
	02H	Set all palette registers and overscan register.	
	03H	Toggle intensity/blinking bit.	
	04H-06H	Reserved.	
	07H	Read individual palette register.	
	08H	Read overscan register.	
	09H	Read all palette registers and overscan.	
	10H	Set individual color register.	
	11H	Reserved.	
	12H	Set block of color registers.	
	13H	Select color page number (not valid in mode 13).	
	14H	TVGA Refresh Control Register	
	15H	Read individual color register.	
	16H	Reserved.	
	17H	Read block of color registers.	
	18H-19H	Reserved.	
	1AH	Read color page state.	
	1BH	Sum color values to gray shades.	
11H		Character generator.	EGA, VGA
	00H	Load user font.	



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Function	Sub-function	Description	Adapter
	01H	Load ROM 8 x 14 font.	
	02H	Load ROM 8 x 8 font.	
	03H	Set block specifier.	
	04H	Load 8 x 16 font.	VGA
	05H	Load ROM 8 x 11 font.	
	10H	Load user font.	
	11H	Load ROM 8 x 14 font.	
	12H	Load ROM 8 x 8 font.	
	14H	Load 8 x 16 font.	VGA
	15H	Load ROM 8 x 11.	
	20H	Set user graphics character pointer at INT 1FH.	
	21H	Set user graphics character pointer at INT 43FH.	
	22H	ROM 8 x 14 font.	
	23H	ROM 8 x 8 font.	
	24H	Load 8 x 16 font.	VGA
	25H	Load ROM 8 x 11 font.	
	30H	Font information.	
12H		Alternate select.	EGA, VGA
	10H	Return VGA information.	
	11H	Return TGUI BIOS information.	
	12H	Return TGUI video memory size.	
	20H	Select alternate print screen routine.	
	30H	Select scan lines for alphanumeric modes.	
	31H	Default palette loading during set mode.	
	32H	Video active.	
	33H	Summing to gray shades.	
	34H	Cursor emulation.	
	35H	Display switch.	
	36H	Video screen on/off.	
13H		Write string.	EGA, VGA
1AH		Read/write display combination code.	VGA
	00H	Read.	



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Function	Sub-function	Description	Adapter
	01H	Write.	
1BH		Return functionality/state information.	VGA
1CH		Save/restore video state.	VGA
	00H	Request save/restore state buffer size.	
	01H	Save state in state buffer.	
	02H	Restore state from saved state buffer.	
1DH		Reserved.	

2.3.6.2. 10h Function: 00H—Set Video Mode

Entry	AH = 00H. AL = Video mode to set. (See below.)
Return	For TGUI standard modes (0-13H): None. For TGUI enhanced modes (50-61H): AH = 00H Set mode successfully. 80H Fail. Wrong switch setting. 81H Insufficient video memory.

Table 2-7 Standard Mode Support

Mode	Type	Color	Alpha Format	Cell Size	Screen Format
0, 1	Text	16	40x25	8x8	320x200
0*, 1*	Text	16	40x25	8x14	320x350
0+, 1+	Text	16	40x25	9x16	360x400
2,3	Text	16	80x25	8x8	720x200
2*, 3*	Text	16	80x25	8x14	640x350
2+, 3+	Text	16	80x25	9x16	720x400
4,5	Graphics	4	40x25	8x8	320x200
6	Graphics	4	80x25	8x8	640x200
7	Text	4	80x25	9x14	720x350
7+	Text	4	80x25	9x16	720x400
D	Graphics	16	40x25	8x8	320x200
E	Graphics	16	80x25	8x8	640x200
F	Graphics	4	80x25	8x14	640x350
10	Graphics	16	80x25	8x14	640x350
11	Graphics	2	80x30	8x16	640x480



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Mode	Type	Color	Alpha Format	Cell Size	Screen Format
12	Graphics	16	80x30	8x16	640x480
13	Graphics	256	40x25	8x8	320x200

2.3.6.3. 10h Function: 01H—Set Cursor Type

Entry	AH = 01H CH: Top line for cursor (bit 4 - 0) CL: Bottom line (bit 4 - 0)
Return	None

2.3.6.4. 10h Function: 02H—Move Cursor

Entry	AH = 02H BH: Page DH: Row of new cursor position DL: Column of new cursor position
Return	None

2.3.6.5. 10h Function: 03H—Get Cursor Location/Type

Entry	AH = 03H BH: Page
Return	(CH, CL) - Cursor type (DH, DL) - (row, column)

2.3.6.6. 10h Function: 04H—Reserved

2.3.6.7. Function: 05H—Select Active Page

Entry	AH = 05H AL: Page number to select
Return	None

2.3.6.8. 10h Function: 06H—Scroll Window Up

Entry	AH = 06H AL: Number of blanked lines at bottom of window AL = 00H will blank entire window BH: Attribute for blank lines (CH, CL): (row, column) of upper left corner (DH, DL): (row, column) of lower right corner
Return	None

Note: The window must be in the active page.



2.3.6.9. 10h Function: 07H—Scroll Window Down

Entry	AH = 07H AL: Number of lines blanked at top of window AL = 00H will blank entire window BH: Attribute for blank lines (CH, CL): (row, column) of upper left corner (DH, DL): (row, column) of lower right corner
Return	None

Note: The window must be in the active page.

2.3.6.10. 10h Function: 08H—Read Character/Attribute at Current Cursor Position

Entry	AH: 08H BH: Page
Return	AH: Attribute of character AL: Character read

2.3.6.11. 10h Function: 09H—Write Character/Attribute to Current Cursor Position

Entry	AH = 09H AL: Character code BH: Page background color for mode 13H BL: Attribute/color of character CX: Character count
Return	None

Note: For graphics mode, except mode 13H, if bit 7 of BL is set, then the color logic value is OR with the color of the current character.

2.3.6.12. 10h Function: 0AH—Write Characters to Current Cursor Position

Entry	AH = 0AH AL: Character code BH: Page CX: Character count
Return	None

2.3.6.13. 10h Function: 0BH—Set Color Palette

10h Function: 0BH - Sub-function: 00H—Set Color Palette

Entry	AH = 0BH BL: Color value to be used BH: Sub-function code BH = 00H Set border color for text modes Set background color for 320 x 200 graphics modes Set foreground color for 640 x 200 graphics mode BL: (0 - 31) BH = 01H Select palette for 320 x 200 graphics
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	BL = 0 Green (1)/red (2)/brown (3) 1 Cyan (1)/magenta (2)/white (3)
Return	None

2.3.6.14. 10h Function: 0CH—Write Dot

Entry	AH = 0CH AL: Color value BH: Page (CX, DX): (row, column) of dot
Return	None

2.3.6.15. 10h Function: 0DH—Read Dot

Entry	AH = 0DH BH: Page (CX DX): (row, column)
Return	AL: Dot read

2.3.6.16. 10h Function: 0EH—Write TTY to Active Page

Entry	AH = 0EH AL: Character Code BL: Foreground color in graphics mode
Return	None

2.3.6.17. 10h Function: 0FH—Read Video State

Entry	AH = 0FH
Return	AH: Maximum character columns AL: Current video mode BH: Current active page

2.3.6.18. 10h Function: 10H—Set Palette Registers

10h Function 10H—Sub-function: 00H—Set Individual Palette Register

Entry	AH = 10H AL = 00H (set individual palette register) BH: Value to set BL: Palette register to set
Return	None

10h Function: 10H—Sub-function: 01H—Set Overscan Register

Entry	AH = 10H AL = 01H (set overscan register) BH: Value to set
-------	--



Return	None
--------	------

10h Function: 10H—Sub-function: 02H—Set All Palette Registers and OverScan Register

Entry	AH = 10H AL = 02H (set all palette registers and overscan registers) (ES:DX): Pointer to a 17-byte table (16 palette registers and 1 overscan register)
Return	None

10h Function: 10H—Sub-function: 03H—Toggle Intensity/Blinking Bit

Entry	AH = 10H AL = 03H (toggle intensity/blinking attribute bit) BL = 0 Enables intensity 1 Enables blinking
Return	None

10h Function: 10H—Sub-function: 04H-06H—Reserved**10h Function: 10H—Sub-function: 07H—Read Individual Palette Register**

Entry	AH = 10H AL = 07H (read individual palette register) BL: Palette to read
Return	BH: Value read

10h Function: 10H—Sub-function: 08H—Read Overscan Register

Entry	AH = 10H AL = 08H (read overscan register)
Return	BH: Value read

10h Function: 10H—Sub-function: 09H—Read All Palette Registers and OverScan

Entry	AH = 10H AL = 09H (read all palette registers and overscan) (ES:DX): Pointer to input buffer. (17 bytes)
Return	(ES:DX): Pointer to input buffer with data

10h Function: 10H—Sub-function: 10H—Set Individual Color Register

Entry	AH = 10H AL = 10H (set individual color register) BX: Set color register DH: Set red value CH: Set green value CL: Set blue value
Return	None.

**10h Function: 10H—Sub-function: 11H—Reserved****10h Function: 10H—Sub-function: 12H—Set Block of Color Registers**

Entry	AH = 10H AL = 12H (set block of color registers) BX: First color register CX: Number of color registers to set (ES:DX): Pointer to table of color values (R,G,B; R,G,B;...)
Return	None

10h Function: 10H—Sub-function 13H—Select Color Page Number (Not Valid for Mode 13)

Entry	AH = 10H AL = 13H (select color page number - not valid for mode 13) BL = 00H Select paging mode BH - Paging mode: = 00H Selects 4 register blocks of 64 registers = 01H Selects 16 register blocks of 16 registers BL = 01H Select Page BH - Page number: For 64-reg block mode: = 00H Select first block of 64 color registers = 01H Select second block of 64 color registers = 02H Select third block of 64 color registers = 03H Select fourth block of 64 color registers For 16-reg block mode: = 00H Select first block of 16 color registers = 01H Select second block of 16 color registers = 0FH Select 16th block of 16 color registers
	None.

Note: After setting video mode, the BIOS is in 64-reg block mode and the first block is active.

10h Function: 10H—Sub-function 15H—Read Individual Color Register

Entry	AH = 10H AL = 15H (read individual color register) BX: Color register to read
Return	DH: Read red value CH: Read green value CL: Read blue value

10h Function: 10H—Sub-function 16H—Reserved**10h Function: 10H—Sub-function 17H—Read Block of Color Registers**

Entry	AH = 10H AL = 17H (read block of color registers) BX: First color register to read CX: Number of color registers to read (ES:DX): Pointer to destination table for values
-------	---



Return	(ES:DX): Pointer to table of values
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10h Function: 10H—Sub-function: 18-19H—Reserved

10h Function: 10H—Sub-function: 1AH—Read Color Page State

Entry	AH = 10H AL = 1AH (read color page state)
Return	BH: Current page BL: Current paging mode

10h Function: 10H—Sub-function: 1BH—Sum Color Values to Gray Shades

Entry	AH = 10H AL = 1BH (sum color values to gray shades) BX: First color register to sum CX: Number of color registers to sum
Return	None

2.3.6.19. 10h Function: 11H—Character Generator

10h Function: 11H—Sub-function: 00H—Load User Font

Entry	AH = 11H AL = 00H (load user font) BH: Bytes per character BL: Block to load CX: Character count DX: Character to be loaded into table (ES:BP): Pointer to user font table
Return	None

10h Function: 11H—Sub-function: 01H—Load ROM 8 x 14 Font

Entry	AH = 11H AL = 01H (load ROM 8 x 14 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 02H—Load ROM 8 x 8 Font

Entry	AH = 11H AL = 02H (load ROM 8 x 8 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 03H—Set Block Specifier

Entry	AH = 11H AL = 03H (set block specifier [valid in alpha modes]) BL: Character generator block selects
-------	--



	Bits 4, 1, 0 select block for characters with attribute bit 3 = 0 Bits 5, 3, 2 select block for characters with attribute bit 3 = 1
Return	None

10h Function: 11H—Sub-function: 04H—Load 8 x 16 Font

Entry	AH = 11H AL = 04H (load 8 x 16 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 05H—Load ROM 8 x 11 Font

Entry	AH = 11H AL = 05H (load ROM 8 x 11 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 10H—Load User Font

Entry	AH = 11H AL = 10H (load user font) BH: Bytes per character BL: Block to load CX: Character count DX: Character into table (ES:BP) : Pointer to user font table
Return	None

10h Function: 11H—Sub-function: 11H—Load ROM 8 x 14 Font

Entry	AH = 11H AL = 11H (load ROM 8 x 14 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 12H—Load ROM 8 x 8 Font

Entry	AH = 11H AL = 12H (load ROM 8 x 8 font) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 14H—Load 8 x 16 Font

Entry	AH = 11H AL = 14H (load 8 x 16 font) BL: Block to load
Return	None



10h Function: 11H—Sub-function: 15H—Load ROM 8 x 11

Entry	AH = 11H AL = 15H (load ROM 8 x 11) BL: Block to load
Return	None

10h Function: 11H—Sub-function: 20H—Set User Graphics Character Pointer at INT 1FH

Entry	AH = 11H AL = 20H (set user graphics character pointer at INT 1FH) (ES:BP) : Pointer to the user table
Return	None

10h Function: 11H—Sub-function: 21H—Set User Graphics Character Pointer at INT 43FH

Entry	AH = 11H AL = 21H (set user graphics character pointer at INT 43FH) BL: Rows specifier = 00H - user CX: Points DL: Rows = 01H - 14 = 02H - 25 = 03H - 30 (ES:BP) : Pointer to user table
Return	None

10h Function: 11H—Sub-function: 22H—ROM 8 x14 Font

Entry	AH = 11H AL = 22H (ROM 8 x 14 font) BL: Row specifier
Return	None

10h Function: 11H—Sub-function: 23H—ROM 8 x 8 Font

Entry	AH = 11H AL = 23H (ROM 8 x 8 font) BL: Row specifier
Return	None

10h Function: 11H—Sub-function: 24H—Load 8 x 16 Font

Entry	AH = 11H AL = 24H (load 8 x 16 font) BL: Row specifier
Return	None

**10h Function: 11H—Sub-function: 25H—Load ROM 8 x 11 Font**

Entry	AH = 11H. AL = 25H (load ROM 8 x 11 font) BL: Row specifier
Return	None

Note: To load a given font, AL = 10H, 11H 12H, 14H, 15H, 20H, 21H, 22H 23H, 24H, or 25H should be called immediately after setting mode function call (AH = 0).

10h Function: 11H—Sub-function: 30H—Font Information

Entry	AH = 11H AL = 30H (tint information) BH: Request font pointer = 00H: Current INT 1FH = 01H: Current INT 43H = 02H: ROM 8 x 14 = 03H: ROM 8 x 8 = 04H: ROM 8 x 8 (top) = 05H: ROM 9 x 14 alternate = 06H: ROM 8 x 16 = 07H: ROM 9 x 16 alternate = 08H: ROM 8 x 11
Return	CX: Bytes per character DL: Row screen size less one (ES:BP): Pointer to font

2.3.6.20. 10h Function: 12H—Alternate Select

10h Function: 12H—Sub-function: 10H—Return VGA Information

Entry	AH = 12H BL = 10H (Return VGA information)
Return	BH = 00H - Color mode in effect 01H - Monochrome mode in effect BL: Video memory size: = 00H 64KB = 01H 128KB = 02H 192KB = 03H 256KB CH: Adapter bits CL: Switch setting

10h Function: 12H—Sub-function: 11H—Return TGUI BIOS Information

Entry	AH = 12H BL = 11H (return TGUI BIOS information)
Return	(ES:BP): Pointer to BIOS version information table with format as follows: = 0000 word OEM_CODE



	= 0002 word version number
BL =	10H BIOS check OK
AL =	12H function supported

10h Function: 12H—Sub-function: 20H—Select Alternate Print Screen Routine

Entry	AH = 12H BL = 20H (select alternate print screen routine)
Return	None

10h Function: 12H—Sub-function: 30H—Select Scan Lines for Alphanumeric Modes

Entry	AH = 12H BL = 30H (select scan lines for alphanumeric modes) AL = 0 - 200 scan line 1 - 350 scan lines 2 - 400 scan lines
Return	AL = 12H (function supported)

10h Function: 12H—Sub-function: 31H—Default Palette Loading During Set Mode

Entry	AH = 12H BL = 31H (default palette loading during set mode) AL = 00H Enable 01H Disable
Return	AL = 12H (function supported)

10h Function: 12H—Sub-function: 32H—Video Active

Entry	AH = 12H BL = 32H (video active) AL = 00H Enable video 01H Disable video
Return	AL = 12H (function supported)

10h Function: 12H—Sub-function: 33H—Summing to Gray Shades

Entry	AH = 12H BL = 33H (summing to gray shades) AL = 00H Enable summing 01H Disable summing
Return	AL = 12H (function supported)

10h Function: 12H—Sub-function: 34H—Cursor Emulation

Entry	AH = 12H BL = 34H (cursor emulation) AL = 00H - Enable emulation 01H - Disable emulation
Return	AL = 12H (function supported)

**10h Function: 12H—Sub-function: 35H—Display Switch**

Entry	AH = 12H BL = 35H (display switch) AL = 00H - Initial adapter video off (ES:DX): Pointer to state save buffer (128 bytes) 01H - Initial system board video on 02H - Switch off active video (ES:DX): Pointer to state save buffer 03H - Switch on inactive video (ES:DX): Pointer to previously saved state buffer
Return	AL = 12H (function supported)

10h Function: 12H—Sub-function: 36H—Video Screen On/Off

Entry	AH = 12H BL = 36H (video screen on/off) AL = 00H On 01H Off
Return	AL = 12H (function supported)

2.3.6.21. 10h Function: 13H—Write String

Entry	AH = 13H (ES:BP): Pointer to string CX: Character count only (control character not included) (DH, DL): (Row, column) begin BH: Page AL = 00H cursor not moved BL: Attribute String format: (char,char,char,...) AL = 01H moved cursor BL: Attribute String format: (char,char,char,...) AL = 02H cursor not moved String format: (char,attr,char,attr,char,attr,...) AL = 03H moved cursor String format: (char,attr,char,attr,char,attr,...)
Return	None.

2.3.6.22. 10h Function: 1AH—Read/Write Display Combination Code**10h Function: 1AH—Sub-function: 00H—Read**

Entry	AH = 1AH AL = 00H (read)
Return	AL = 1AH (function supported) BH: Alternate display code



	BL: Active display code
--	-------------------------

10h Function: 1AH—Sub-function: 01H—Write

Entry	AH = 1AH AL = 01H (write) BH: Alternate display code BL: Active display code
Return	AL = 1AH (function supported) Display code table: 00H : No display 01H : Monochrome with 5151 02H : CGA with 5153/4 (color) 03H : Reserved 04H : EGA with 5153/4 (color) 05H : EGA with 5151 (mono) 06H : Professional graphics system with 5175 (color) 07H : PS/2 except M30 with analog monochrome 08H : PS/2 except M30 with analog color 09H : Reserved 0AH: Reserved 0BH: PS/2 M30 analog monochrome 0CH: PS/2 M30 analog color 0DH-FEH : Reserved FFH : Reserved

2.3.6.23. 10h Function: 1BH—Return Functionality/State Information

Entry	AH = 1BH BX = 00H (ES:DS): Pointer to user buffer (64 bytes) for return of information																																																						
Return	AL = 1BH (function supported) Information returned to user: <table><tr><th>Offset</th><th>Length</th><th></th></tr><tr><td>00H</td><td>word</td><td>Offset to static functionality information</td></tr><tr><td>02H</td><td>word</td><td>Segment to static functionality information</td></tr><tr><td>04H</td><td>byte</td><td>Video mode</td></tr><tr><td>05H</td><td>word</td><td>Columns on screen</td></tr><tr><td>07H</td><td>word</td><td>Length of regenerator buffer (bytes)</td></tr><tr><td>09H</td><td>word</td><td>Starting address in regenerator buffer</td></tr><tr><td>0BH</td><td>word</td><td>Cursor position for 8 pages (row, col)</td></tr><tr><td>1BH</td><td>word</td><td>Cursor type (start/end)</td></tr><tr><td>BH</td><td>byte</td><td>Active display page</td></tr><tr><td>1BH</td><td>word</td><td>CRT controller address</td></tr><tr><td>20H</td><td>byte</td><td>Current setting for 3 x 8 register</td></tr><tr><td>21H</td><td>byte</td><td>Current setting for 3 x 9 register</td></tr><tr><td>22H</td><td>byte</td><td>Rows on screen</td></tr><tr><td>23H</td><td>word</td><td>Character height (scan lines/char)</td></tr><tr><td>25H</td><td>byte</td><td>Display combination code (active)</td></tr><tr><td>26H</td><td>byte</td><td>Display combination code (alternate)</td></tr><tr><td>27H</td><td>word</td><td>Colors supported for current video mode</td></tr></table>	Offset	Length		00H	word	Offset to static functionality information	02H	word	Segment to static functionality information	04H	byte	Video mode	05H	word	Columns on screen	07H	word	Length of regenerator buffer (bytes)	09H	word	Starting address in regenerator buffer	0BH	word	Cursor position for 8 pages (row, col)	1BH	word	Cursor type (start/end)	BH	byte	Active display page	1BH	word	CRT controller address	20H	byte	Current setting for 3 x 8 register	21H	byte	Current setting for 3 x 9 register	22H	byte	Rows on screen	23H	word	Character height (scan lines/char)	25H	byte	Display combination code (active)	26H	byte	Display combination code (alternate)	27H	word	Colors supported for current video mode
Offset	Length																																																						
00H	word	Offset to static functionality information																																																					
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04H	byte	Video mode																																																					
05H	word	Columns on screen																																																					
07H	word	Length of regenerator buffer (bytes)																																																					
09H	word	Starting address in regenerator buffer																																																					
0BH	word	Cursor position for 8 pages (row, col)																																																					
1BH	word	Cursor type (start/end)																																																					
BH	byte	Active display page																																																					
1BH	word	CRT controller address																																																					
20H	byte	Current setting for 3 x 8 register																																																					
21H	byte	Current setting for 3 x 9 register																																																					
22H	byte	Rows on screen																																																					
23H	word	Character height (scan lines/char)																																																					
25H	byte	Display combination code (active)																																																					
26H	byte	Display combination code (alternate)																																																					
27H	word	Colors supported for current video mode																																																					



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	29H	byte	Pages supported for current video mode
	2AH	byte	Scan lines in current mode = 0 - 200 = 1 - 350 = 2 - 400 = 3 - 480
	2BH	byte	Primary character block
	2CH	byte	Secondary character block
	2DH	byte	Miscellaneous state information: bits 7, 6 Reserved bit 5 = 0/1 Intensity/blinking bit 4 = 1 Cursor emulation active bit 3 = 1 Default palette loading disabled bit 2 = 1 Monochrome display attached bit 1 = 1 Summing active bit 0 = 1 All modes in display active
	2EH-30H	Reserved	
	31H	byte	Video memory available: 0, 1, 2, 3 - 64k, 128k, 192k, 256k
	32H	byte	Save pointer state information: bits 7, 6 Reserved bit 5 = 1 DCC extension active bit 4 = 1 Palette override active bit 3 = 1 Graphics font override active bit 2 = 1 Alpha font override active bit 1 = 1 Dynamic save area active bit 0 = 1 512-character set active
	33H-3FH	Reserved	
	Format of static functionality table:		
	Offset	Length	
	00H	byte	Supported mode flags for modes 07H-00H
	01H	byte	Supported mode flags for modes 0FH-08H
	02H	byte	Supported mode flags for modes 013H-10H
	03H-06	Reserved	
	07H	byte	Scan lines available in text modes: bit 3: 480 lines bit 2: 400 lines bit 1: 350 lines bit 0: 200 lines
	08H	byte	Character blocks available
	09H	byte	Maximum number of active character blocks
	0AH	byte	Miscellaneous functions: bit 7: Color paging (see AH10) bit 6: Color palette (see AH10) bit 5: EGA palette (see AH10) bit 4: Cursor emulation bit 3: Default palette loading bit 2: Font loading bit 0: All modes on all display
	0BH	byte	Miscellaneous functions: bit 7-4 Reserved



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		bit 3:	DCC (see AH1A)
		bit 2:	Intensity/blinking control
		bit 1:	Save/restore (see AH1C)
		bit 0:	Light pen
	0CH-0DH	Reserved	

	0EH	byte	Save pointer functions:
			bit 7, 6: Reserved
			bit 5: DCC extension
			bit 4: Palette override
			bit 3: Graphics font override
			bit 2: Text font override
			bit 1: Dynamic save area
			bit 0: 512 character set
	0FH	byte	Reserved

2.3.6.24. 10h Function: 1CH—Save/Restore Video State

10h Function: 1CH—Sub-function: 00H—Request Save/Restore State Buffer Size

Entry	AH = 1AH AL = 00H (request save/restore state buffer size) CX: Requested states: bits 15-3: Reserved and set to 0 bit 2 = 1 Save/restore video DAC state and color registers bit 1 = 1 Save/restore video BIOS data bit 0 = 1 Save/restore video hardware state
Return	AL = 1CH Function supported BX: Required buffer size block count. 64-byte per block.

10h Function: 1CH—Sub-function: 01H—Save State in State Buffer

Entry	AH = 1AH AL = 01H (save state in state buffer) CX = Requested states (ES:BX): Pointer to save state buffer
Return	AL = 1CH Function supported

10h Function: 1CH—Sub-function: 02H—Restore State from Saved State Buffer

Entry	AH = 1AH AL = 02H (restore state from saved state buffer) CX: Requested states (ES:BX): Pointer to state buffer
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Return	AL = 1CH Function supported
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2.3.7. Extended Int 10h Calls

The following interrupt calls have been added to the interrupt list.

2.3.7.1. Int 10h Function: 12h—Sub-function: 12H—Return TGUI Video Memory Size

The Volari XP10 BIOS has a function call for measuring the video memory size. This information can easily be obtained by making a BIOS function call 12h and Sub-function call 12h. The following table shows the handshaking for this call:

Entry	AH = 12H BL = 12H (return TGUI video memory size)
Return	AH: Video memory value: = 01H, 256KB = 02H, 512KB = 03H, 768KB = 04H, 1024KB = 05H, 2048KB = 06H, 4096KB = 07H, 2.5MB = 08H, 6MB = 0AH, 8MB = 0CH, 10MB = 0EH, 12MB = 10H, 14MB = 12H, 16MB

2.3.7.2. Int 10h Function: 12h—Sub-function: 13H—Return BIOS function

Entry	AH= 12h (Alternate select) BL= 13h (Sub-function)
Return	AH= 'x' in ASCII format AL= 12h (Success) BX= 'NT' in ASCII format CH= CC in BCD format CL= cc in BCD format DH= MM in BCD format DL= mm in BCD format SI= 'xX' in ASCII format DI= 'ss' in ASCII format

**2.3.7.3. Int 10h Function: 12h—Sub-function: 14H—Set Mode**

Entry	AH= 12h (Alternate select) BL= 14h (Sub-function) AL= 00h (<i>Set TVGA extended modes</i>) BH= Mode number as listed in this specification CL= Refresh Rate Real Value as listed in this specification in binary For example: for 70Hz enter 46h. CH= Mode specifier D6 1: Linear address enable D4 1: Set CRT2 timing only D3-D1 000: 16 color 001: 256 color 010: 32k color 011: 64k color 100: True color D0 Reserved
Return	AH= 00h (function successful) 81h (Mode not supported because the mode requested is not in the list defined in this BIOS specification.) AL= Actual refresh rate set

If there is insufficient memory during this function call, the error code will be returned and the last mode will be kept.



2.3.7.4. Int 10 Function 10h Sub-function 14h Call for TVGA Refresh Control

10h Function: 10H - Sub-function 14H — TVGA Refresh Control Register

INT 10H	Sub Function 14 (00) Set TVGA Refresh Rate Mode (01) Get Mode Refresh Rates (0A) Get Attached Display Device Information (0B) Proof of Current Display Status (0C) Expansion Control (0D) Display switching control (0E) TV Standard Switching
---------	---

	(AH) = 12H, (BL) = 14H (AL) = 01H				INT 10H sub-function entry Sub-function Get Mode Refresh Rate			
Input	(BH) = TVGA Mode Number							
Output	(AH) = 00H : passed, otherwise failed							
	Refresh Rate Index: (IN = interlaced)							
	(BH)							
	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	Reserved	100	85	80	75
	(BL)							
	7	6	5	4	3	2	1	0
	72	70	65	60	56	96 IN	87IN	Reserved

	(AH) = 12H, (BL) = 14H (AL) = 0AH				10H sub-function entry Sub-function Get Monitor Information			
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Input	BH = 00H (Get attached display device information) 01H (DVI monitor hot plug/unplug hook – called by system BIOS) CX = D0 LCD D1 CRT D2 TV (Reserved) D3 DVI CL = 0 Unplugged (When BH = 01) 1 Plugged (When BH = 01)
Output	(AH) = 00H : OK, Otherwise failed (CH) D7 2 nd display 0: Not present; 1: Display attached D6 2 nd display type if D7 is '1' 0: Analog; 1: Digital D5 – D4 Attached CRT display 00: Not present; 01: Color display; 10: Mono display; 11: Unknown D1 – D0 LCD display 00: Not present; 01: Present (TFT); 10: Present (DSTN); 11: Reserved

	(AH) = 12H, (BL) = 14H (AL) = 0BH	10H sub-function entry Sub-function Proof Current Display
	Function: Set 3CF_5B bits 0, 1, and 2 according to actual display status.	
Input	None	
Output	None	

	(AH) = 12H, (BL) = 14H (AL) = 0CH	10H sub-function entry Sub-function Expansion Control
	Function: Set the expansion status in 3CF.5d and load the new LCD CRTC parameter on the fly in LCD mode.	
Input	(BH) = 0H (Get Panel Info)	
Output	(AH) = 00H: OK, Otherwise Failed (CL) Expansion status 00H = Centering; 01H = Expansion	



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Input	(BH) = 1H (Set expansion status) (CL) Expansion status 00H = Centering; 01H = Expansion
Output	(AH) = 00H: OK; otherwise failed (CL) Expansion status 00H = Centering; 01H = Expansion

	(AH) = 12H, (BL) = 14H (AL) = 0DH	10H sub-function entry Sub-function Output control
	Function: Control the display output to different device	
Input	(BH) = 0H (Get current display device)	
Output	(AH) = 00H : OK, otherwise failed (CL) Display device D0 = LCD; D1 = CRT; D2 = TV; D3 = DVI	
Input	(BH) = 1H (Set output device) (CL) Display device D0 = LCD; D1 = CRT; D2 = TV; D3 = DVI	
Output	(AH) = 00H : OK, otherwise failed (CL) Display device D0 = LCD; D1 = CRT; D2 = TV; D3 = DVI	
Input	(BH) = 2H (Turn on/off LCD) (CL) 00H = Off; 01H = On;	
Output	(AH) = 00H : OK, otherwise failed	
Input	(BH) = 3H (Device switch pre-hook in Windows) (CL) Display device D0 = LCD; D1 = CRT; D2 = TV;	
Output	(AH) = 00H : OK, otherwise failed	



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Input	(BH) = 4H (Device switch post-hook and update CMOS in Windows) (CL) Display device D0 = LCD; D1 = CRT; D2 = TV;
Output	(AH) = 00H : OK, otherwise failed

	(AH) = 12H, (BL) = 14H	10H sub-function entry
	(AL) = 0EH	Sub-function PAL/NTSC control
	Function: TV Format Control (NTSC/PAL)	
Get NTSC/PAL switching capability		
Input	(BH) = 0H	
Output	(AH) = 00H: Capable of switching between NTSC/PAL on the fly = 81H: Switching between NTSC/PAL not supported	
Set NTSC/PAL		
Input	(BH) = 1H (CL) = 0H: NTSC 1H: PAL	
Output	(AH) = 00H : OK, otherwise failed	
Enable/Disable TV		
Input	(BH) = 2H (CL) = 00H: Disabled 01H: Enabled	
Output	(AH) = 00H : OK, otherwise failed (CL) = 00H: NTSC 01H: PAL	
Get TV scanning status		
Input	(BH) = 3H	
Output	(AH) = 00H : OK, otherwise failed (CL) = D0: 0 = Underscan mode; 1 = Overscan mode D4: 1 = Native TV mode	
Set TV scanning status		
Input	(BH) = 4H (CH) = D0: Valid bit 0 of CL D4: Valid bit 4 of CL	



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	(CL) = D0: 0 = Underscan mode; 1 = Overscan mode D4: 1 = Native TV mode
Output	(AH) = 00H : OK, otherwise failed

	(AH) = 12H, (BL) = 14H (AL) = 0FH	10H sub-function entry Sub-function Re-Post
	Function: Executes post	
Input	(AH) = 12H (BL) = 14H (AL) = 0FH	
Output	None	

	(AH) = 12H, (BL) = 14H (AL) = 10H	10H sub-function entry Sub-function Mode 3 Special Service
	Function: Mode 3 Special Service	
Input	(AH) = 12H (BL) = 14H (AL) = 10H (BH) = 00H: Save mode 3 first page data and font data 01H: Restore mode 3 first page data and font data 02H: Set mode 3 that clears first page only ES:DI = Buffer address to save/restore data	
Output	None	

	(AH) = 12H, (BL) = 14H (AL) = 80H	10H sub-function entry Sub-function Get TV Information
	Function: Get TV support information (encoder)	
Input	(BH) = 00H	
Output	(AH) = 12H: Old chip (analog TV/non-TV) 00H: Digital TV encoder (BX) = 02H: Trident TVXress2 chip is present	
	Function: Get TV support information	
Input	(BH) = 01H	



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Output	(AH) = 12H: Old chip (analog TV/non-TV) 00H: Digital TV encoder 80H: Cannot auto-detect (AL) = 0xH: No TV connected 1xH: TV connected (Composite) 4xH: TV connected (S-Video) 5xH: TV connected (both) 2xH: Cannot auto-detect
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	(AH) = 12H, (BL) = 14H (AL) = 90H	10H sub-function entry Sub-function Misc. Services
	Function: Get BIOS capability and LCD timing parameters	
Input	(AH) = 12H (BL) = 14H (AL) = 90H	
Output	(AH) = 00H: OK, otherwise failed (BX) = High word of BIOS capability (DX) = Low word of BIOS capability (CX) = Number of LCD parameters (ES:DI) = Pointer of LCD parameters for native resolution	

	(AH) = 4FH, (AL) = 15H	10H sub-function entry Sub-function I2C Access
	Function: Write I2C	
Input	(BL) = 50H: Write EDID (CL) = Data to be written (CH) = I2C port number (don't care if it is internal TV) D0: GPIO (reserved) D1: 1 st I2C D2: Reserved D3: 2 nd I2C (DL) = I2C address (DH) = I2C index	



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Output	(AX) = Status
	Function: Read I2C
Input	(BL) = 60H: Read EDID (CH) = I2C port number (don't care if it is internal TV) D0: GPIO (reserved) D1: 1 st I2C D2: Reserved D3: 2 nd I2C (DL) = I2C address (DH) = I2C index
Output	(AX) = Status (CL) = Data



2.4. Extended Functionality

In addition to the VBE function calls, the Volari XP10 provides a wealth of other useful function calls.

2.4.1. Physical Detection of Volari XP10

I/O register 3C5 index 9 can be accessed directly to see if the attached device is the Volari XP10. The following table displays the register definition:

Table 2-8 Register Definition

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Definition
3C5.9	0	0	0	0	0	0	0	1	Device is Volari XP10 Rev. A
3C5.9	0	0	0	0	0	0	1	0	Device is Volari XP10 Rev. B
3C5.9	0	0	0	0	0	0	1	1	Device is Volari XP10 Rev. C

2.4.2. Variable Refresh Rate Support

For CRT only:

640x400:	70 and 85Hz
640x480:	60, 75, 85, 100 and 120Hz
800x600:	60, 75, 85, 100 and 120Hz
1024x768:	87i, 60, 75, 85, 100 and 120Hz
1280x1024:	87i, 60, 75, 85 and 100Hz
1600x1200:	96i, 60, 75, 85 and 100Hz
1920x1440	60Hz
2048x1536	60Hz

For LCD support following refresh rate for different panels in all available modes:

- LCD display is limited by the memory bandwidth available.

2.4.3. Memory Clock Selection

Table 2-9 MCLK Speeds (in MHz) selected by pins GPIO6 and GPIO5

GPIO6	GPIO5	CLOCK
0	0	200
0	1	250
1	0	275



1	1	300
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2.4.4. Wake-up and Sleep Mechanism

The Volari XP10 can be put to sleep and awakened by making a direct access to the register 3C3h as shown in Table 2-14.

Table 2-10 Wake-up/Sleep Mechanism

Function	Register	Bit 0	Description
Sleep	3C3h	0	Volari XP10 is disabled
Wake up	3C3h	1	Volari XP10 is enabled



3. Standard VGA Registers

The standard VGA register sets include Sequencer Registers, Graphics Controller Registers, Attribute Registers, CRT Controller Registers, and VGA General Registers. In the descriptions that follow, all reserved bits are read back as 0 unless otherwise specified.

3.1. Sequencer Address Register

Address: 3C4H Access: Read/Write

Register Access: This register is accessed directly through its port address.

Bits 7:4 Reserved

Bits 3:0 Sequencer Address Bits. A binary value that points to the register from which data is to be written or read.

Bit	3	2	1	0	
	0	0	0	0	Reset Register
	0	0	0	1	Clocking Mode Register
	0	0	1	0	Map Mask Register
	0	0	1	1	Character Map Select Register
	0	1	0	0	Sequencer Memory Mode Register

Note: This register is loaded with a binary value that points to the sequencer data register from which data is to be written or read. This value is referred as "Index".

3.2. Reset Register

Address 3C5H Index: 00 Access: Read/Write

Register Access: To access this register, the index value is first written to 3C4. Port 3C5 is then used for one read or write operation.

Bits 7:2 Reserved.

Bit 1 Synchronous Reset. If memory contents are to be preserved, reset the sequencer with this bit before changing the Clocking mode Register. Bits 1 and 0 must both be ones to allow the sequencer to operate:

- 0: Requests the sequencer to synchronously clear and halt *
- 1: Requests the sequencer to run when bit 0 of this register is non-zero

Bit 0 Asynchronous Reset. Resetting the sequencer with this bit can cause data loss in the dynamic RAMs:

- 0: Requests the sequencer to asynchronously clear and halt
- 1: Requests the sequencer to run when bit 1 of this register is non-zero



3.3. Clocking Mode Register

Address: 3C5H Index: 01 Access: Read/Write

Register Access: To access this register, the index value is first written to 3C4. Port 3C5 is then used for one read or write operation.

- Bits 7:6 Reserved.
- Bit 5 Screen off. This bit can be used to update screen. When this bit is set, the screen is blanked and the sync pulses continue to drive the monitor:
0: Selects normal screen operation.
1: Turns off the video screen and assigns maximum bandwidth to the CPU.
- Bit 4 Shift 4. This bit overrides the value programmed in bit 2. This mode is useful when 32 bits are fetched per cycle and chained together in the shift registers:
0: The video serializers are loaded every character clock.
1: The serializers are loaded every fourth character clock.
- Bit 3 Dot Clock. Dot clock divided by two is used for modes 0H, 0*H, 0+H, 1H, 1*H, 1+H, 4H, and 5H to provide 40 columns of characters. All other timing will be stretched since it is derived from the dot clock:
0: Selects normal dot clocks derived from the sequencer master clock input.
1: The master clock is divided by 2 to generate the dot clock.
- Bit 2 Shift Load. This mode is useful when 16 bits are fetched per cycle and chained together in the shift registers:
0: When Bit 4 is also 0, serializers are reloaded every character clock. When Bit 4 is 1, Bit 2 has no effect.
1: When Bit 4 is 0, serializers are loaded every other character clock.
- Bit 1 Reserved.
- Bit 0 8/9 Dot Clocks. VGA modes of 0+H, 1+H, 2+H, 3+H, 7+H, and CGA mode 7+H use the 9 dot character clock. All other modes use the 8 dot character clock. If the Attribute Mode Controller Register bit 2 is set, the 9th dot will match the 8th dot for ASCII character codes in the range of C0H to DFH. For all other characters the 9th dot will match the background color:
0: Directs the sequencer to generate clocks 9 dots wide.
1: Directs the sequencer to generate clocks 8 dots wide.

3.4. Map Mask Register

Address: 3C5H Index: 02 Access: Read/Write

Register Access: To access this register, the index value is first written to 3C4. Port 3C5 is then used for one read or write operation.

- Bits 7:4 Reserved.



Bits 3:0 Map Mask

- 1: Enables the processor to write to the corresponding maps 3 through 0. If this register has the value of hex 0F, the CPU can perform a 32-bit write operation with only one memory cycle.

This substantially reduces the overhead on the CPU during display update cycles in graphics modes. Data scrolling operations are also enhanced by setting this register to a value of hex 0F and writing the display buffer address with the data stored in the CPU data latches. This is a read-modify-write operation. When chain 4 mode is selected, all maps should be enabled.

3.5. Character Map Select Register

Address: 3C5H Index: 03 Access: Read/Write

Register Access: To access this register, the index value is first written to 3C4. Port 3C5 is then used for one read or write operation.

Bits 7:6 Reserved

Bits 5, 3:2 Character Map Select A. Bits 5, 3, and 2 select another character map offset as follows:

Bit 5 3 2	Map Select	Addr Offset into Map #2
0 0 0	0	0
0 0 1	1	16K
0 1 0	2	32K
0 1 1	3	48K
1 0 0	4	8K
1 0 1	5	24K
1 1 0	6	40K
1 1 1	7	56K

Bits 4, 1:0 Character Map Select B. Bits 4, 1, and 0 select a character map offset as follows:

Bit 4 1 0	Map Select	Addr Offset into Map #2
0 0 0	0	0
0 0 1	1	16K
0 1 0	2	32K
0 1 1	3	48K
1 0 0	4	8K
1 0 1	5	24K
1 1 0	6	40K
01 1 1	7	56K

- a)
 1. In alphanumeric modes, bit 3 of the attribute byte normally has the function of turning the fore-ground intensity on or off. This bit, however, may be redefined as a switch between character sets. For this feature to be enabled, the following must be true:
 2. Sequencer memory Mode register (3C5.04) bit 1 must be a logical 1.
 3. The value of Character Map Select A must not equal the value of Character Map Select B.



3.6. Sequencer Memory Mode Register

Address: 3C5H Index: 04 Access: Read/Write

Register Access: To access this register, the index value is first written to 3C4. Port 3C5 is then used for one read or write operation.

Bits 7:4 Reserved

Bit 3 Chain 4:

- 0: Enables processor addresses to access data within a bitmap by use of the Sequencer Map Mask Register.
- 1: Causes the two low order bits to select the map which will be accessed during processor memory operations.

A1	A0	Map Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even:

- 0: Directs even processor addresses to access maps 0 and 2, while odd processor addresses access maps 1 and 3.
- 1: Causes the processor addresses to access data within a bitmap.

Bit 1 Extended memory:

- 0: If the total memory installed is 64K.
- 1: Enables the TGUI to access the 256K of memory available.

Bit 0 Reserved

4. Standard VGA Graphics Controller Registers

These sets of Standard VGA registers format the data sent from the CPU to the Video Display Memory by programming the set/reset register, bit rotation, and functions select (AND, OR, or XOR) depending on the application. In addition, a color comparison operation can be performed when the CPU requests data from the Video Display Memory.

4.1. Graphics Address Register

Address: 3CEH Access: Read/Write

Register Access: This register is accessed directly through its port address.

Bits 7:4 Reserved

Bits 3:0 Graphics Address Bits

4.2. Set/Reset Register

Address: 3CFH Index: 00 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bits 7:4 Reserved

Bits 3:0 Sets (logical 1)/Resets (logical 0) all 8 bits of Map 0 - Map 3 respectively during a type 0 memory write. The operation can be masked for each map by programming the Enable Set/Reset Register (index of Hex 01).

4.3. Enable Set/Reset Register

Address: 3CFH Index: 01 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bits 7:4 Reserved.

Bits 3:0 Enable Set (logical 1)/Reset (logical 0). Bits may be masked in each plane. This is accomplished by "ANDing" rotated CPU data and the Bit Mask Register. If the mode register is programmed to Write Mode 0, then the contents of the Set/Reset Register are written to the respective display memory planes. If the Write Mode is 0 and Set/Reset is not enabled for a given plane, the plane is written with the data from the CPU data bus.

4.4. Color Compare Register

Address: 3CFH Index: 02 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bits 7:4 Reserved

Bits 3:0 Color compare. These are reserved for a 4-bit color value to be compared when the system microprocessor does a type 1 memory read. The Color Don't Care Register (index 07H) is used to control the comparison of each map.

4.5. Data Rotate Register

Address: 3CFH Index: 03 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bits 7:5 Reserved

Bits 4:3 Function select:

Bit	4	3
0 0:	CPU Data unchanged.	
0 1:	CPU Data ANDed with latched data.	
1 0:	Data ORed with latched data.	
1 1:	CPU Data XORed with latched data.	

Bits 2:0 Rotate Count. Rotate operation is active when the CPU writes to the display memory and when the write mode is 0. These bits represent the number of positions to right-rotate the CPU data.

4.6. Read Map Select Register

Address: 3CFH Index: 04 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bits 7:2 Reserved

Bits 1:0 Map Select. These bits represent the map from which the system microprocessor reads data when the read mode is 0 and the memory mode is not chain 4 mode. This register does not effect the color compare read mode.

4.7. Graphics Mode Register

Address: 3CFH Index: 05 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

Bit 7 Reserved

Bit 6 256 Color Mode:

- 0: Bit 5 controls the loading of the shift registers.
- 1: Shift registers support the 256 color mode.

Bit 5 Shift Register:

- 0: Standard shift register operation
- 1: Directs the shift registers to format the serial data with even-numbered or odd-numbered bits from even/odd-numbered maps

- Bit 4 Odd/Even:
 0: Read data sequentially from planes
 1: Used to emulate CGA (Color Graphics Adapter) modes
- Bit 3 Read Mode:
 0: Read Mode 0
 1: Read Mode
- Bit 2 Reserved
- Bits 1:0 Write Mode:
 Bit 1 0
 0 0: Write Mode 0
 0 1: Write Mode 1
 1 0: Write Mode 2
 1 1: Write Mode 3

4.8. **Miscellaneous Register**

Address: 3CFH Index: 06 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

- Bits 7:4 Reserved
- Bits 3:2 Memory Map. Controls the mapping of the regenerative buffer to the CPU address space:
 Bit 3 2
 0 0: A0000H for 128K bytes
 0 1: A0000H for 64K bytes
 1 0: B0000H for 32K bytes (mono)
 1 1: B8000H for 32K bytes (color)
- Bit 1 Odd/Even:
 0: Standard Addressing
 1: Replaces CPU address bit 0 with a higher-order bit and selects odd-even maps according to the odd/even value of the CPU A0 bit
- Bit 0 Graphics Mode. This bit controls alphas-mode addressing:
 0: Selects alpha-mode
 1: Selects graphics mode

Note: When bits 3:2 = 11B, registers 3D8 and 3D9 are enabled.

4.9. **Color Don't Care Register**

Address: 3CFH Index: 07 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

- Bits 7:4 Reserved

- Bit 3 Color Plane 3:
 0: Don't Care for color compare cycle
 1: Utilize the color compare cycle
- Bit 2 Color Plane 2:
 0: Don't Care for color compare cycle
 1: Utilize the color compare cycle
- Bit 1 Color Plane 1:
 0: Don't Care for color compare cycle
 1: Utilize the color compare cycle
- Bit 0 Color Plane 0:
 0: Don't Care for color compare cycle
 1: Utilize the color compare cycle

4.10. Bit Mask Register

Address: 3CFH Index: 08 Access: Read/Write

Register Access: To access this register, the index value is first written to 3CE. Port 3CF is then used for one read or write operation.

- Bits 7:0 Bit Mask:
 0: Immune to change
 1: Allows unimpeded writes to the corresponding bits in the maps

5. Standard VGA Attribute Controller Registers

The Standard VGA Attribute Controller registers perform operations such as color select, screen panning control, attribute mode change, overscan color select, and color plane enable.

5.1. Attribute Address Register

Address: 3C0H Access: Read/Write

Register Access: This register is accessed directly through its port address.

Bits 7:6 Reserved

Bit 5 Palette Address Source:
0: Allows CPU to load the addressed palette registers
1: Normal operation

Bits 4:0 Attribute Address Bits. Point to the attribute data register where data is to be written. Since the Attribute Address Register and data registers have the same write port address, an internal flip-flop is used to select the address register or data registers. This flip-flop is reset to point to the address register whenever the system CPU reads port 3BAH or 3DAH. When the flip-flop is set, it points to the data registers from which a target register can be specified by the index in the Attribute Address Register. This flip-flop will toggle after each I/O write to port hex 3C0H. I/O read will not affect this flip-flop.

5.2. Palette Register

Address: 3C0H, 3C1H Index: 00-0F Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

Bits 7:6 Reserved

Bits 5:0 Palette. These bits allow a dynamic mapping between the text attribute or graphics color input value and the display color on the CRT screen.

5.3. Attribute Mode Control Register

Address: 3C0H, 3C1H Index: 10 Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

- Bit 7** P5, P4 Select. Selects the source for the P5 and P4 digital video bits:
- 0: Selects Bit 5 and Bit 4 of Palette Registers to go off chip as P5 and P4 respectively
 - 1: Selects Bit 1 and Bit 0 of Color Select Register to go off chip as P5 and P4 respectively
- Bit 6** PEL Width:
- 0: Always 0 (except for 256-color modes)
 - 1: Directs Attribute Controller to support 256 color modes
- Bit 5** PEL Panning Compatibility. This bit allows a selected portion of the screen to be panned:
- 0: No effect on the PEL Panning register output
 - 1: Forces the PEL Panning register output to 0 until vertical retrace occurs
- Bit 4** Reserved
- Bit 3** Enable Blink/Select Background Intensity:
- 0: Selects the background intensity (text mode) or color attribute (graphics mode)
 - 1: Activates the blink attribute
- Bit 2** Enable Line Graphics Character Codes:
- 0: Ninth dot of the line graphics character will be the same as background
 - 1: Activates the line graphics character codes for monochrome emulation mode
- Bit 1** Mono Emulation:
- 0: Sets color emulation mode
 - 1: Sets monochrome emulation mode
- Bit 0** Graphics/Alphanumeric Mode:
- 0: Selects alphanumeric mode
 - 1: Selects graphics mode

5.4. Overscan Color Register

Address: 3C0H, 3C1H Index: 11 Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

Bits 7:0 Overscan Color. These bits are used to determine the overscan color displayed on the CRT screen.

5.5. Color Plane Enable Register

Address: 3C0H, 3C1H Index: 12 Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

Bits 7:6 Reserved

Bits 5:4 Video Status MUX. Selects two of the eight color outputs for the status port. The selected color outputs can then be read by Input Status Register One (Read Port 3xAH), bits 4 and 5.

Input Status Register:

Bit 5 4	Bit 5	Bit 4	
0 0	P2	P0	P0 = Blue
0 1	P5	P4	P1 = Green
1 0	P3	P1	P2 = Red
1 1	P7	P6	P3 = Secondary Blue
			P4 = Secondary Green
			P5 = Secondary Red

Bit 3 Color Plane 3 Enable: 0: Disable; 1: Enable

Bit 2 Color Plane 2 Enable: 0: Disable; 1: Enable

Bit 1 Color Plane 1 Enable: 0: Disable; 1: Enable

Bit 0 Color Plane 0 Enable: 0: Disable; 1: Enable

5.6. Horizontal PEL Panning Register

Address: 3C0H, 3C1H Index: 13 Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/ 3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

Bits 7:4 Reserved

Bits 3:0 Horizontal PEL Panning. Selects the number of PELs to be shifted left.

5.7. Color Select Register

Address: 3C0H, 3C1H Index: 14 Access: Read/Write

Port: Write: 3C0H Read: 3C1H

Register Access: To access this register, port 3DAH or 3BAH (depending on display) is read to set the flag to index location. The index is then written to 3C0H (write operation)/ 3C1 (read operation). Data is then read from port 3C1H for a read operation and written to port 3C0H for a write operation.

Bits 7:4 Reserved

Bits 3:2 S_color 6-7. Form the 8-bit digital color value sent off-chip. (except for 256 color modes)

Bits 1:0 S_color 4-5. Form the 8-bit digital color value sent off-chip. See Attribute Mode Control Register Bit 7.

6. Standard VGA CRT Controller Registers

The CRT Controller Registers control the CRT by generating the blanking and syncing signals to define the display raster. The screen display data format is also defined by these registers.

6.1. CRT Controller Address Register

Address: 3B4H, 3D4H Access: R/W

Port: Mono Display, 3B4H
Color Display, 3D4H

Register Access: This register is accessed directly through its port address.

Bits 7:6 Reserved

Bits 5:0 CRT Controller Address Bits. A binary value pointing to the CRT Controller Register where data is to be written or read.

Note: The location of the CRT Controller Address Register (3B4H or 3D4H) depends on Bit 0 of the Miscellaneous Output Register, located at 3C2H.

6.2. Horizontal Total Register

Address: 3B5H, 3D5H Index: 00 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Horizontal Total. The total number of characters less 5.

Note: This register defines the total number of characters in the horizontal scan interval including the retrace time.

6.3. Horizontal Display Enable End Register

Address: 3B5H, 3D5H Index: 01 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Horizontal Display Enable End. Total number of displayed characters per horizontal line less one.

Note: This address register defines the length of the horizontal display enable signal, and determines the number of displayed character positions per horizontal line.

6.4. Start Horizontal Blanking Register

Address: 3B5H, 3D5H Index: 02 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Start Horizontal Blanking. The horizontal blanking signal becomes active when the horizontal character counter reaches this value.

6.5. End Horizontal Blanking Register

Address: 3B5H, 3D5H Index: 03 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bit 7 Reserved

Bits 6:5 Display Enable Skew Control. These bits determine the amount of display enable skew:

Bit 6 5

0 0: No skew

0 1: Shift left one character

1 0: Shift left two characters

1 1: Shift left three characters

Bits 4:0 End Horizontal Blanking. This signal is disabled when the six least significant bits of the horizontal character counter equal this value. Bit 5 is located in the End Horizontal Retrace Register (index 05H). The 6-bit result to be programmed into this register equals the value of the Start Blanking Register plus the width of the blanking signal in character clock units.

6.6. Start Horizontal Retrace Pulse Register

Address: 3B5H, 3D5H Index: 04 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Start horizontal Retrace Pulse. The value programmed is a binary count of the character position number at which the signal becomes active.

Note: Used to center the screen horizontally and to specify the character position when the Horizontal Retrace Pulse becomes active.

6.7. End Horizontal Retrace Register

Address: 3B5H, 3D5H Index: 05 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bit 7 End Horizontal Blanking, Bit 5. Bit 5 of a 6-bit value. Bits 4-0 are located in the End Horizontal Blanking Register.

Bits 6:5 Horizontal Retrace Delay. These two bits control the skew of the horizontal retrace signal:

Bit 6	5
0 0:	No CLK delay
0 1:	Shift left one CLK
1 0:	Shift left two CLKs
1 1:	Shift left three CLKs

Bits 4:0 End Horizontal Retrace. The horizontal retrace signal is disabled when the value of these bits is equal to the five least-significant bits of horizontal character counter value. The 5-bit value to be programmed into this register equals the value of the Start Horizontal Retrace Register plus the width of the Horizontal Retrace Signal in the character clock unit.

Note: Used to specify the character position at which the Horizontal Retrace Pulse becomes inactive.

6.8. Vertical Total Register

Address: 3B5H, 3D5H Index: 06 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Vertical Total. These are the lower-order 8 bits of a 10-bit register. Bits 8 and 9 are located at bits 0 and 5 of the CRT Controller Overflow Register (index 07H), respectively. The value in this register is the number of horizontal raster scan lines on the CRT screen minus two, including vertical retrace.

6.9. CRT Controller Overflow Register

Address: 3B5H, 3D5H Index: 07 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

- Bit 7 Vertical Retrace Start. Bit 9 of the 10-bit Vertical Retrace Start Register.
- Bit 6 Vertical Display Enable End. Bit 9 of the 10-bit Vertical Display Enable End Register.
- Bit 5 Vertical Total. Bit 9 of the 10-bit Vertical Total Register.
- Bit 4 Line Compare. Bit 8 of the 10-bit Line Compare Register.
- Bit 3 Start Vertical Blank. Bit 8 of the 10-bit Start Vertical Blank Register.
- Bit 2 Vertical Retrace Start. Bit 8 of the 10-bit Vertical Retrace Start Register.
- Bit 1 Vertical Display Enable End. Bit 8 of the 10-bit Vertical Display Enable End.
- Bit 0 Vertical Total. Bit 8 of the 10-bit Vertical Total Register.

6.10. Preset Row Scan Register

Address: 3B5H, 3D5H Index: 08 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

- Bit 7 Reserved

Bits 6:5 Byte Panning Control. Bits 5 and 6 control byte panning, and can be used in conjunction with the Pel Panning Register.

Bits 4:0 Preset Row Scan. This register specifies the starting row scan count after a vertical retrace.

Note: Used for PEL scrolling.

6.11. Maximum Scan Line Register

Address: 3B5H, 3D5H Index: 09 Access: Read/Write

Port: Mono Display, 3B5H
 Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bit 7 200 to 400 Line Conversion. This allows 200 line modes to be displayed as 400 lines on the monitor.

Bit 6 Line Compare. Bit 9 of the 10-bit Line Compare Register

Bit 5 Start Vertical Blank. Bit 9 of the 10-bit Start Vertical Blank

Bits 4:0 Maximum Scan Lines. This register specifies the number of scan lines per character row.

6.12. Cursor Start Register

Address: 3B5H, 3D5H Index: 0A Access: Read/Write

Port: Mono Display, 3B5H
 Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:6 Reserved

Bit 5 Cursor ON/OFF:
 0: Turns on the cursor
 1: Turns off the cursor

Bits 4:0 Cursor Start. This register specifies the row scan of a character line at which the cursor is to begin.

6.13. Cursor End Register

Address: 3B5H, 3D5H Index: 0B Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bit 7 Reserved

Bits 6:5 Cursor Skew. These bits control the skew of the cursor signal:

Bit 6 5

0 0: No skew

0 1: Shift left one character

1 0: Shift left two characters

1 1: Shift left three characters

Bits 4:0 Cursor End. These bits specify the row scan at which the cursor is to end.

6.14. Start Address High Register

Address: 3B5H, 3D5H Index: 0C Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Start Address. High order 8 bits of the start address.

Note: Also see Start Address Low Register 3D5.0D. For bit 16 of the Start Address see 3D5.1E. For bits 19-17 see 3D5.27.

6.15. Start Address Low Register

Address: 3B5H, 3D5H Index: 0D Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Start Address. Low order 8 bits of the Start Address.

b) 1. Bit 16 of Start Address is located in the CRTC Module Testing Register (3X5.1E, bit5).

2. Also see Start Address High Register 3D5.0C. For bit 16 of the Start Address see 3D5.1E. For bits 19-17 see 3D5.27.

6.16. Cursor Location High Register

Address: 3B5H, 3D5H Index: 0E Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Cursor Location. High order 8 bits of the Cursor Location.

6.17. Cursor Location Low Register

Address: 3B5H, 3D5H Index: 0F Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Cursor Location. Low order 8 bits of the Cursor Location.

6.18. Vertical Retrace Start Register

Address: 3B5H, 3D5H Index: 10 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Vertical Retrace Start. Lower 8 bits of the 10-bit Vertical Retrace Start Register. The start position is programmed in horizontal scan lines. Bit 8 is located at bit 2 of the CRTC Controller Overflow Register (index 07H). Bit 9 is located at bit 7 of the CRTC Controller Overflow Register (index 07H).

6.19. Vertical Retrace End Register

Address: 3B5H, 3D5H Index: 11 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

- Bit 7 Protect R[7:0]. The Line Compare bit in the CRTC Overflow Register is not affected by this protect bit:
0: Enables writes to CRTC registers [7:0]
1: Disables writes to CRTC registers [7:0]
- Bit 6 Select 5 Refresh Cycles:
0: Generates 3 DRAM refresh cycles per horizontal line
1: Generates 5 DRAM refresh cycles per horizontal line
- Bit 5 Enable Vertical Interrupt:
0: Enables vertical interrupt. The Vertical interrupt is on IRQ2.
1: Disables vertical interrupt
- Bit 4 Clear Vertical Interrupt:
0: Clears a vertical interrupt
1: No effect
- Bits 3:0 Vertical Retrace End. When the vertical retrace output signal is disabled, these bits determine the horizontal scan count value. The 4-bit value to be programmed into the register equals the value of the Start Vertical Retrace register plus the width of the Vertical Retrace signal in the horizontal scan unit.

6.20. Vertical Display Enable End Register

Address: 3B5H, 3D5H Index: 12 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

- Bits 7:0 Vertical Display Enable End. This address is used to specify which scan line ends the active video area of the screen. These bits are the low-order 8 bits of the 10-bit vertical display enable end position value. (Bits 8 and 9 are located at bit 1 and bit 6, respectively, of the CRTC Controller Overflow Register.)

6.21. Offset Register

Address: 3B5H, 3D5H Index: 13 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Offset. This register is used to specify the logical line width of the screen. It is programmed with word address offset. This means the offset is multiplied by 2 before it is added to the starting address of the previous character row. Extended Bit 8 is located at bit 4 of the Address and Color mode register (3X5.29).

6.22. Underline Location Register

Address: 3B5H, 3D5H Index: 14 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bit 7 Reserved

Bit 6 Double Word Mode:
1: Memory address is the double word address

Bit 5 Count by 4. This bit is used when double word addresses are employed:
0: Memory address counter clocked by character clock
1: Memory address counter clocked by x/4 character clock. Double word addresses only.

Bits 4:0 Underline Location. This register is used to specify the horizontal row scan.

6.23. Start Vertical Blanking Register

Address: 3B5H, 3D5H Index: 15 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Start Vertical Blank. These are the lower 8 bits of the horizontal scan line count at which the vertical blanking signal becomes active. Bit 8 of the scan count is located at bit 3 in the CRTC Overflow Register. Bit 9 is located at bit 5 in the Maximum Scan Line Register.

6.24. End Vertical Blanking Register

Address: 3B5H, 3D5H Index: 16 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 End Vertical Blank. This 8-bit register specifies the horizontal scan count value at which vertical blanking is inactive. The 8-bit value equals the value of Start Vertical Blanking Register less one, plus the width of the Vertical Blank signal in horizontal scan units.

6.25. CRTC Mode Control Register

Address: 3B5H, 3D5H Index: 17 Access: Read/Write

Port: Mono Display, 3B5H
Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

- Bit 7 Hardware Reset:
0: Resets horizontal and vertical retrace
1: Enables horizontal and vertical retrace
- Bit 6 Word/Byte. When bit 6 of underline location register is 0, this bit selects word/byte mode:
0: Word mode
1: Byte mode
- Bit 5 Address Wrap. This bit selects Memory Address counter 13 (logical 0) or 15 (logical 1). The given bit appears on the MA0 output pin when in the word address mode.
- Bit 4 Horizontal Retrace Select. Doubles the vertical resolution of the CRT Controller:
0: Selects Horizontal Retrace
1: Selects Horizontal Retrace divided by 2
- Bit 3 Count by Two:
0: The memory address counter is clocked with the character clock input.
1: Clocks the memory address counter with the character clock input divided by 2.
- Bit 2 Horizontal Retrace Select. Doubles the vertical resolution of the CRT Controller:
0: Selects Horizontal Retrace
1: Selects Horizontal Retrace divided by 2
- Bits 1 Select Row Scan Counter:
0: Selects row scan counter bit 1 on MA 14 output pin
1: Selects MA 14 counter bit on MA 14 output pin

- Bit 0 Compatibility Mode Support:
- 0: During active display time, row scan address bit 0 is substituted for memory address bit 13.
 - 1: Enables memory address bit 13 to appear on the memory address output bit 13 signal of the CRT Controller.

6.26. Line Compare Register

Address: 3B5H, 3D5H Index: 18 Access: Read/Write

Port: Mono Display, 3B5H
 Color Display, 3D5H

Register Access: To access this register, the index value is first written to 3B4 or 3D4. Port 3B5 or Port 3D5 is then used for one read or write operation.

Bits 7:0 Line Compare. Lower 8 bits of the compare target. Bit 8 is in the CRT Controller Overflow Register (index 7). Bit 9 is in the Maximum Scan Line Register (index 9). A successful line compare will reset the internal address counter which supports split screen display. Therefore, the screen display with starting address of Hex 0000H will not be affected by scrolling.

7. Standard VGA General Registers

This set of registers has its own port addresses, and they can be accessed directly without an index and data register.

7.1. Miscellaneous Output Register

Address: 3C2H, 3CCH Access: Read/Write

Port: Write: 3C2H
Read: 3CCH

Register Access: This register is accessed directly through its port address.

Bit 7 Vertical SYNC Polarity:
0: Positive vertical retrace
1: Negative vertical retrace
Bit 76 Vertical Size
00: Reserved
01: 400 lines
10: 350 lines
11: 480 lines

Bit 6 Horizontal SYNC Polarity:
0: Positive horizontal retrace
1: Negative horizontal retrace

Bit 5 Page bit for Odd/Even, selects between two 64K pages of memory when in the Odd/Even modes (1H-5H):
0: Selects low page of memory
1: Selects high page of memory

Bit 4 Reserved

Bits 3:2	3C2, bit 3 or 3DB, bit 3	3C2, bit 2 or 3DB, bit 0	Clock Frequency (MHz)
	0	0	25.175
	0	1	28.322
	1	0	Programmable*
	1	1	36.000

Note: *Programmable via registers 3C5.18 and 3C5.19

Bit 1 Enable RAM:
0: Disables video RAM
1: Enables video RAM

Bit 0 I/O Address Select:
0: Sets CRTC address to 3BxH and Input Status Register 1 address to hex 3BA (for Monochrome emulation).
1: Sets CRTC address to 3DxH and Input Status Register 1 address to hex 3DA (for Color Graphics emulation).

Note: The vertical size of the monitor is encoded using the polarity of the sync signals.

7.2. Input Status Register 0

Address: 3C2H Access: RO

Register Access: This register is accessed directly through its port address.

- Bit 7 CRT Interrupt:
 - 0: Vertical retrace interrupt is cleared
 - 1: Vertical retrace interrupt is pending
- Bits 6:5 Reserved
- Bit 4 Switch Sense. Determines whether a monochrome or color monitor is connected:
 - 0: Monochrome
 - 1: Color
- Bits 3:0 Reserved

7.3. Input Status Register 1

Address: 3XAH Access: RO

Register Access: This register is accessed directly through its port address.

- Bits 7:6 Reserved
- Bits 5:4 Diagnostic Usage. These two bits are selectively connected to two of the eight color outputs of the Attribute Controller. The Color Plane Enable register controls the selection of which two color outputs are read.

Color Plane Register	Input Status Register One		
Bit 5 4	Bit 5 4		
0 0	P2	P0	P0 = blue
0 1	P5	P4	P1 = green
1 0	P3	P1	P2 = red
1 1	P7	P6	P3 = secondary blue
			P4 = secondary green
			P5 = secondary red

- Bit 3 Vertical retrace:
 - 0: Video information is being displayed on the CRT screen.
 - 1: CRT is in a vertical retrace interval.
- Bits 2:1 Reserved
- Bit 0 Display Enable NOT. This bit is the logical negative of the real-time status of the display enable signal.
 - 1: CRT raster in a horizontal or vertical retrace interval

Note: The colors are indicated only to provide correlation with compatible modes. They become meaningless when the display DAC color values are modified from their default settings.

8. Standard VGA Setup Registers

These are the two Standard VGA video enable ports on the XP10. XGI's Video BIOS defaults to 3C3H.

8.1. Video Subsystem Enable Register

Address: 3C3H Access: Read/Write

Register Access: This register is accessed directly through its port address.

Bits 7:1 Reserved

Bit 0 Video subsystem:

0: Disable video I/O and memory address decoding

1: Enable video I/O and memory address decoding

8.2. Display Adapter Enable Register

Address: 46E8H Access: Read/Write

7	6	5	4	3	2	1	0
Reserved				Display Adapter	Reserved		

Register Access: This register is accessed directly through its port address.

Bits 7:4 Reserved

Bit 3 Display adapter:

0: Disable video I/O and memory address decoding

1: Enable video I/O and memory address decoding

Bits 2:0 Reserved

9. Extended Mode Register Description

In the descriptions that follow, all of the reserved bits are read back as 0 unless otherwise specified. Please see Reset MD Configuration Table for latest mapping of reset configuration options.

9.1 Old New Status Register

Address: 3C5H Index: 08 Access: Read Only

Bit 7	Status: 0: old 1: new
Bit 6	Even (1)/Odd(0) field of interface scan
Bit 5	Reserved
Bit 4	Command FIFO empty (active low)
Bits 3:0	Reserved

9.2. Revision Control Register

Address: 3C5H Index: 09 Access: Read Only

Bits 7:0	Version number Reset: TBD
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9.3. Reserved

Address: 3C5H Index: 0A Access: Read/Write

9.4. Version and Old/New Mode Control Register

Address: 3C5H Index: 0B Access: Read/Write

Bits 7:0	An I/O write will change Old/New Mode Control Register (3C5.0DH, 3C5.0EH & 3CF.0EH) to the old definition. An I/O read will change Old/New Mode Control Register to the new definition. Reset: F3H
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9.5. Configuration Port Register 1

Address: 3C5H Index: 0C Access: Read/Write

This register is enabled by 3C5.0E_old bit 5 = 1, and 3C5.0E_new bit 7 = 1. Read from this register is enabled by 3C5.OE_OLD bit 5 = 0

Bit 7	Reserved
Bit 6	1: 64-bit memory bus

- Bit 5 Reserved (Shall be read 1)
- Bit 4 Video Subsystem enable:
 - 0: 46E8
 - 1: 3C3
- Bit 3 BIOS Size:
 - 0: 64K
 - 1: 32K
- Bit 2 Reserved
- Bits 1:0 Reserved
 - Reset: 101(MD13)(MD12)111b

9.6. Configuration Port Register 2

Address: 3C5H Index: 0C Access: Read/Write

Write to this register is enabled by 3C5.0E_old bit 5 = 0.

- Bits 7:0 Reserved for BIOS
 - Reset: NA

9.7. Old Mode Control Register 2

Address: 3C5H Index: 0D Access: Read/Write

- Bits 7:4 Reserved (Bit [5] read 1)
- Bit 3 CPU bandwidth select:
 - 0: normal
 - 1: non-interrupted CPU access during VBLANK
- Bits 2:0 Reserved (Read 0)
 - Reset: 20h

9.8. New Mode Control Register 2

Address: 3C5H Index: 0D Access: Read/Write

- Bits 7:4 Display FIFO threshold control:
 - 0000: 2 level
 - 0001: 4 level
 - 0010: 6 level
 - 0011: 8 level
 - 0100: 10 level
 - 0101: 12 level
 - 0110: 14 level
 - 0111: 16 level
 - 1000: 18 level
- Bit 3 Enable display memory clock divided by 2 (active high)

- Bits 2:1 Video clock divide control:
 00: divide by 1
 01: divide by 2
 10: divide by 4
 11: divide by 1.5
- Bit 0 Reserved
 Reset: 10h

9.9. Old Mode Control Register 1

Address: 3C5H Index: 0E Access: Read/Write

- Bit 7 Reserved (read 1)
- Bit 6 IRQ polarity select:
 0: active high
 1: active low
- Bit 5 Configuration port (3C5.0C) select:
 0: select port 2
 1: select port 1
- Bit 4 Reserved
- Bit 3 Reserved (Read back as 1)
- Bits 2:1 256k bank select:
 00: bank 0
 01: bank 1
 10: bank 2
 11: bank 3

An inverted value will write into bit 1.

- Bit 0 Invert Pixel Clock to RAMDAC:
 0: Normal;
 1: Invert pixel clock to RAMDAC (default 0)

When values of 3CF.06 bits [3:2] equal 00, bits [2:1] of this register and bit 5 of 3C2 will be enabled. Bit 5 of 3C2 is used as page select register to select one of the two 64K bytes pages.
 Reset: A8h

9.10. New Mode Control Register 1

Address: 3C5H Index: 0E Access: Read/Write

- Bit 7 Configuration port (3C5.0C, 3C5.0F, 3X5.28, 3X5.29, 3X5.2A, & bit [6:4] of this register) write enable (active high)
- Bit 6 Reserved

Bits 5:0 64K bank select (total of 64 banks for 4MB memory)

(Note: bit 1 should be inverted when performing write)

Bits [5:0] of this register are enabled by writing to register bits [3:2] of 3CF.06 with a value other than 00.

Reset: 40h

9.11. Power-up Mode Register 2

Address: 3C5H Index: 0F Access: Read/Write

Bit 7 Reserved

Bit 6 BIOS Control:
1: enabled
0: disabled

Bit 5 Palette mode:
1: Intel retry mode
0: master abort mode

Bit 4 Linear/Bank Addressing Control:
0: Linear Only
1: Linear/Bank

Bits 3:0 Reserved for BIOS
Reset: 1(MD8)1(MD9)1111b
This register is protected by 3C5.0E_new bit 7.

9.12. VESA Big BIOS Control Register

Address: 3C5H Index: 10 Access: Read/Write

Bit 7 Enable extended VESA Big BIOS: 1: enable; 0: disable (read-only; equivalent to the enable ROM bit in 3C5.F bit 6)

Bits 6:5 Video Address Select:
00: A0000-A7FFF
01: Reserved
10: B0000-B7FFF
11: B8000-BFFFF

These bits are RO and should be decoded from the memory map bits in 3CF.6 bits 2 and 3.

Bits 4:1 Reserved (for future expansion beyond 64K BIOS)

Bit 0 Page Select:
0: Select the original C0000-C7FFF access
1: Select the extended BIOS access defined by bits 6 and 5

Bit [0] of this register is protected by 3C5.0E_NEW bit [7].

9.13. Protection Register

Address: 3C5H Index: 11 Access: Read/Write

- Bits 7:0 Set to 92h to unprotect all extended registers without regard to 3C5.e bit 7.
Set to 87h to unprotect all extended registers except those which may still be protected by 3C5.e bit 7.
Other values protect all extended registers.
Reset: 00h

9.14. Threshold Register

Address: 3C5H Index: 12 Access: Read/Write

- Bits 7:4 Threshold of display queue when both playback or capture is enabled
- Bits 3:0 Threshold of display queue when either playback or capture is enabled.
The old threshold is used when neither playback nor capture is enabled.
All three thresholds can not be set to 0. Other definitions are the same as the original.
Reset: 21h

9.15. Alternative Destination Segment Address

Address: 3D8H Access: R/W

- Bit 7 Reserved
- Bits 6:0 Alternative destination segment address
Reset: 00h
R/W of this register is enabled by 3CF.0F, bit 2.
This register becomes active when 3CF.06, bit [3:2] is not equal to 00.

9.16. Alternative Source Segment Address

Address: 3D9H Access: Read/Write

- Bit 7 Reserved
- Bits 6:0 Alternative source segment address
Reset: N/A
R/W of this register is enabled by 3CF.0F, bit 2.
This register becomes active when 3CF.06, bit [3:2] is not equal to 00.

9.17. Alternate Clock Select Register

Address: 3XBH Access: Read/Write

- Bits 7:5 Same function as new mode control register (3C5.0D) bit [3:1]
- Bits 4:2 Reserved
- Bit 0 Video clock select

9.18. CRT Interlace Control Register

Address: 3X5H Index: 19 Access: Read/Write

Bits 7:0 Interlaced VSYNC adjust values

9.19. CPU Latch Read Back Register

Address: 3D4/3D5H Index: 22 Access: Read Only

Bits 7:0 Latch data pointed by VGA read map select register

9.20. VGA Attribute State Read Back Register

Address: 3X5H Index: 24 Access: RO

Bit 7 0: address; 1: data

Bits 6:0 Other bits are reserved.
Reset: N/A

9.21. RAMDAC R/W Timing Adjust Register

Address: 3X5H Index: 25 Access: Read/Write

Bits 7:0 I/O buffers of PCLK and P[7:0] tri-state control:
0: enable
1: disable

Bits 6:4 Reserved

Bits 3:0 RAMDAC™ R/W wait state
Reset: 000x1111b

9.22. Coarse Register

Address: 3D4/3D5H Index: 26 Access: Read/Write

Bits 7:2 Coarse code input to select coarse delay range. Needs to set SEL_EXT_DELYCTRL to 1.
* Default value is 00000H.

Bits 1:0 Limit coarse delay line working range. Needs to set SEL_EXT_DELYCTRL to 0, and set SEL_CTL_NEW to 1.
* Default value is 0H.

9.23. CRT High Order Start Address Register

Address: 3D4/3D5H Index: 27 Access: Read/Write

Bit 7 Vertical Total bit 10

Bit 6 Vertical blanking start bit 10

Bit 5 Vertical retrace start bit 10

Bit 4 Vertical display enable end bit 10

Bit 3 Line compare bit 10

Reserved

Bits 2:1

Bit 0 PCI linear base address size requested based on the real demand of frame buffer.
 *0: 128MB; 1: 256MB;

9.24. Reserved for S/W definition

Address: 3D4/3D5H Index: 28

9.25. RAMDAC™ Mode Register

Address: 3D4/3D5H Index: 29 Access: Read/Write

Bit 7 Enable external DAC
 0: Disable access to external DAC. *
 1: Enable access to external DAC.

Bits 6:5 SDFBSIZE
 System display frame-buffer size (big page based).
 *0: 0MB; 1: 16MB; 2: 32MB; 3: 64MB

Bit 4 Reserved

Bit 3 Enable GEIO decode

Bit 2 RAMDAC™:
 0: External *
 1: Internal

Bits 1:0 RS[3:2] for RAMDAC™ if register access definition is selected.
 Reset: 0x000000b
 This register is protected by 3C5.0E_NEW bit 7.

9.26. Interface Select Register

Address: 3D4/3D5H Index: 2A Access: Read/Write

Bit 7 Enable Dual 64-bit memory bus
 1: Dual 64-bit memory bus
 0: Single 64-bit memory bus *

Bit 6 Enable internal 32 bit data path:
 1: internal is 32-bit data path
 0: internal is 8/16-bit data path *

Bit 5 EN_SEP_WR
 1: Enable separated Write to Read feature (or called gapless write to read) in GDDRII defined by Samsung.
 *0: no support.

Bit 4 Power Down Select
 1: Enable power down mode using ROMCS# *
 0: Don't power down using ROMCS#

Bit 3 Reserved

- Bit 2 Substitute internal MCLK with PCICLK (for testing only)
 1: Substitute internal MCK with PCICLK
 0: Normal *
- Bits 1:0 Memory Size (The switch point in one linear logic memory space when working along with dual ports of physical memory consists of this logic memory space):
 0: 32 MB *
 1: 64 MB
 2: 128 MB
 3: 256 MB

9.27. Horizontal Parameters Overflow Register

Address: 3D4/3D5H Index: 2B Access: Read/Write

- Bits 7:5 Reserved
- Bit 4 9th bit of Horizontal Blank Start
- Bit 3 9th bit of Horizontal Retrace Start
- Bit 2 9th bit of Horizontal Interlace Parameter
- Bit 1 9th bit of Horizontal Display Enable
- Bit 0 9th bit of Horizontal Total
 Default: 00h

9.28. Memory Controller 0 Register

Address: 3D4/3D5H Index: 2C Access: Read/Write

- Bits 7:6 FIFO Full Watermarker for High Priority Queue in Memory Controller
- 0: 8 levels
 1: 16 levels
 2: 32 levels *
 3: 32 levels
- Bits 5:4 FIFO Full Watermarker for Low Priority Queue in Memory Controller
- 0: 8 levels
 1: 16 levels
 2: 32 levels *
 3: 32 levels
- Bit 3 Enable Prediction mechanism in Memory Controller (Default: 0H)
- Bits 2:0 SDRAM Memory type select
- | | |
|-----------------------------|------------------------------|
| 0: 2M x 32 (4 banks) | 1: 4M x 32/4Mx16 (4 banks) * |
| 2: 8M x 32/8M x16 (4 banks) | 3: 16M x 16 (4 banks) |
| 4: 32M x 16 (4 banks) | 5~7: Reserved |

9.29. General Purpose Register

Address: 3D4/3D5H Index: 2D Access: Read/Write

- Bits 7:0 Reserved

Bit 0

9.30. 2nd I2C Control (1st DVI & 2nd CRT)

Address: 3D4/3D5H Index: 30 Access: Read/Write

Bits 7:4

Bit 3

1: Write

*0: Read

When EPROMWR = 1, SDA is sent to SDO (to display device).

When EPROMWR = 0, SDI (input from display device) is sent to SDA.

Bit 2

Bit 1

2nd^t I2C SCL signal (DDC) (W)

Bit 0

9.31. Read Cache Control Register

Address: 3D4/3D5H Index: 33 Access: Read/Write

Bit 7

0: disable *

1: enable

Bit 6

0: disable *

1: enable

Bits 5:4

Bit 3

1: Enable

*0: Disable

Bits 2:0

9.32. Graphics/Video Engine Control Register

Address: 3D4/3D5H Index: 36 Access: Read/Write

Bit 7	Graphics engine: 1: enabled (3D + 2D) 0: disabled (3D + 2D) *
Bit 6	Reserved
Bit 5	Reserved
Bit 4	GE software reset. Writing a 1 into this bit will reset the graphic engine.
Bit 3	Reserved
Bit 2	ENGE_3D 0: Disable Graphic Engine(3D) * 1: Enable Graphic Engine(3D) ENGE_3D must be valid together with ENGE in order to enable 3D engine finally.
Bits 1:0	Reserved

9.33. I²C Control Register

Address: 3X5H Index: 37 Access: Read/Write

Bit 7	Reserved
Bit 6	1 st I ² C SCL status (RO)
Bit 5	Reserved
Bit 4	2 nd I ² C SCL signal
Bit 3	I ² C operation: 1: write 0: read *
Bit 2	I ² CSEL: 1: Enable 1 st set I ² C 0: Enable 2 nd set I ² C *
Bit 1	I ² C SCL signal (DDC) (W)
Bit 0	I ² C SDA signal (R/W) Reset: 10000010b (bit [2] is protected by 3C5.0e_NEW bit 7)

9.34. Pixel Bus Mode Register

Address: 3X5H Index: 38 Access: Read/Write

- Bit 7 TRIPLE10
 2-10-10-10 Color Mode
 1: Enable
 *0: Disable
- Bit 6 Reserved
- Bit 5 Enable packed 24-bit True Color mode
- Bit 4 In 64-bit configuration, standard VGA mode: 1: enabled; 0: disabled
- Bit 3 True Color mode:
 1: enabled
 0: disabled
- Bit 2 Hi-color mode:
 1: enabled
 0: disabled
- Bit 1 Reserved
- Bit 0 16-bit pixel bus:
 1: enabled
 0: disabled
Reset: 00h

9.35. Misc. Internal Register 1

Address: 3X5H Index: 39 Access: Read/Write

- Bit 7 Pixel data format:
 1: big endian
 0: little endian
- Bits 6:5 When big endian format is used, memory data is:
 11: full swap (fs)
 10: half swap (hs)
 01: word swap (ws)
 00: pass through (pt).
- Bits 4:3 When big endian format is used, BE[3:0]# is:
 11: full swap (fs)
 10: half swap (hs)
 01: word swap (ws)
 00: pass through (pt)
- Bit 2 PCI burst write:
 0: disable
 1: enable

- Bit 1 PCI burst read:
0: disable
1: enable
- Bit 0 MMIO Control:
0: disable
1: enable
- When this bit is 1, which is controlled by an external jumper, the whole 64KB VGA I/O space can be memory mapped within 4GB memory space.
Reset: 0000000(~MD16)
This register is protected by 3C5.0E_new bit 7

9.36. Physical Address Control Register

Address: 3D4/3D5H Index: 3A Access: Read/Write

- Bit 7 Reserved
- Bit 6 AGP/PCI select
0: Select PCI using external IDSEL
1: Select AGP using internal AD16/AD17 as IDSEL *
- Bit 5 Both_IO
0: No MMIO
1: Enable both pure-IO and MMIO *
- Bit 4 SEL_EXT_DELYCTRL
0: Coarse code is controlled by internal logic *
1: Select external coarse code input to set coarse delay line delay
- Bit 3 MDRV
- Bit 2 AGP software reset internally
0 = normal (power-on reset) *
1 = reset
- Bit 1 PCI configuration Subsystem ID write
0 = disable *
1 = enable
- Bit 0 Enhanced register I/O scheme
0 = normal *
1 = enhanced register I/O scheme (3 cycles PCI I/O operation)

9.37. Clock and Tuning Register *(protected by 3C5.0E_new bit 7)*

Address: 3X4H/3X5H Index: 3B Access: Read/Write

- Bit 7 PSDEDO
Observe clock source:
1: LCLK.
*0: VCLK.
- Bit 6 CLKMOD1
1: Select MCK source generated externally.
*0: Select MCK source generated internally.
Reset by MDCONF[0] when chip is powered up.

- Bit 5 CLKMOD0
 *1: Normal operation.
 0: Enable internal clock test mode.
- Bit 4 SELVCK
 Observe clock source:
 1: VCK (source is the result selected by bit7).
 *0: MCLK
- Bit 3 DIV16CK
 Observe clock divided by two:
 1: Divided by two (source is the result selected by bit4).
 *0: Normal condition (not divided by two).
- Bit 2 SEL_HALFCLK
 1: Select half-cycle clock as the observed clock.
 *0: Select MCLK or MCLK2 as the observed clock.
- Bit 1 SEL_MCK2
 1: Select MCLK2 as the observed clock.
 *0: Select MCLK as the observed clock.
- Bit 0 ENVRMR
 Memory refreshing when in vertical retracing.
 *1: Normal condition.
 0: Turn on this feature.

9.38. Misc. Internal Register 2

Address: 3X5H Index: 3C Access: Reserved

- Bits 7:3 Same definition as 3CF.0F[7:3]
 Reserved
- Bit 2 Same definition as 3CF.0F[7:1]
- Bit 1
- Bit 0 Mode select:
 1: original definition of 3CF.0F, bits [7:3] and [1] are accessed by this register only;
 3CF.0F is used to access its bits [2] and [0] only; bit 2 of 3CF.0F now can be
 read and written, but it does not control anything;
 *0: this register does not function; 3CF.0F is used to access bits [7:0] for
 old Trident's compatible products.

9.39. Misc. Internal Register 3

Address: 3D4H/3D5H Index: 3D Access: Read/Write

- Bit 7 Reserved

Bits 6:4 HC2SA<18:16>

The 2nd Hardware starting address bit18 – bit16

3D5.79 and 3D5.78 define starting address bit15 – bit0.

Bit 3 Reserved

Bits 2:0 HCSA<18:16>

The 1st Hardware starting address bit18 – bit16

3D5.45 and 3D5.44 define starting address bit15 – bit0.

*The default value is 00H

9.40. Reserved

Address: 3X5H Index: 3E-3F

9.41. Bus Grant Termination Control Register

Address: 3X4H/3X5H Index: 51 Access: Read/Write

Bit 7 NEWSTOP

*1: Turn on new circuit to lunch PCI STOP signal.

0: Keep the old circuit.

Bit 6 VIP_OFF

1: Turn off VIP feature.

*0: Turn on VIP feature.

Bit 5 IOW_WAIT

1: I/O Write waiting for write buffer empty.

*0: Normal condition.

Bit 4 RDRTY_DISCARD_NUM

1: Wait for 1k clocks to discard an unfinished PCI RETRY operation.

*0: Wait for 32k clocks to discard an unfinished PCI RETRY operation.

Bit 3 Reserved

Bit 2 REG_VSYNCOFF

1: Turn on Surface 0 HSYNC flip instead of VSYNC flip.

*0: Normal condition, only flip when VSYNC.

Bit 1 REG_VSYNCOFF1

1: Turn on Surface 1 HSYNC flip instead of VSYNC flip.

*0: Normal condition, only flip when VSYNC.

Bit 0 REG_VSYNCOFF2

1: Turn on Surface 2 HSYNC flip instead of VSYNC flip.

*0: Normal condition, only flip when VSYNC.

9.42. Reserved

Address: 3X5H Index: 52 Access: Reserved

9.43. Misc. Internal Register 3

Address: 3X5H Index: 54-53 Access: Read/Write

Bits 15:13 Reserved
Bits 12:8 SRCBNK<12:8>
Complement for 3D9
Bits 7:5 Reserved
Bits 4:0 BNKKIT<12:8>
Complement for 3D8

9.44. Misc. Internal Register 4

Address: 3X4H/3X5H Index: 56 Access: Read/Write

Bits 7:5 REG_A12_SEL
Select what will the real A12 on the memory bus.
*0: normally as is (A12); 1: fixed as A11;
2: fixed as BA1; 3: fixed as /BA1;
4: fixed as BA0; 5: fixed as /BA0;
6: fixed as low (1'b0); 7: fixed as high (1'b1);
Bits 4:2 REG_A11_SEL
Select what will the real A11 on the memory bus.
*0: normally as is (A11); 1: fixed as BA1;
2: fixed as /BA1; 3: fixed as BA0;
4: fixed as /BA0; 5: fixed as low (1'b0);
6: fixed as high (1'b1); 7: Reserved
Bits 1:0 REG_BA1_SEL
Select what will the real BA1 on the memory bus. This is only effective when
ONLY2BANK (3D4.5F[1]) is high.
*0: fixed as BA0; 1: fixed as /BA0;
2: fixed as low (1'b0); 3: fixed as high (1'b1);

9.45. Memory Controller 1

Address: 3X5H Index: 5D Access: Read/Write

- Bit 7 REG_QT
To define refresh cycles together with 3X5.2F.bit6 & 3X5.11.bit6 for each horizontal line.
*Default as 0.
- Bit 6 REG128
1: Single 128-bit external DDR memory bus.
*0: Not single 128-bit external DDR memory bus.
This register bit only takes effect when MI_MODE and REG64 are not set.
- Bits 5:1 REG_PIPE_ADJUST
Pipe adjusts between function blocks inside dram controller. In sequence, these 5 bits are controlling:
[5]: DATA_STATUS_TMP
[4]: CMD_ARB
[3]: INPUT_PATH
[2]: OUTPUT_PATH (reserved)
[1]: MEMORY_CONTROLLER
*Default 01100b
- Bit 0 REG64
1: 64-bit external memory bus.
*0: 128-bit external memory bus.

9.46. Test Control Register

Address: 3X5H Index: 5F Access: Read/Write

- Bit 7 TESTOUT
*0: Disable DFT observe port output enable control
1: Enable DFT observe port output enable control
- Bits 6:5 TSTVLNBF, NGETESTSEL0
11: Select debug port to observe Line buffer 96 BIST error and alpha cursor
10: Select debug port to observe TV test out
01: Select debug port to observe Scaling and Fast Overlay
00: Select debug port to observe RGORGB
- Bit 4 REG_NEWIO
*0: Original ping-pang structure of DDR I/O input logic.
1: New relay structure of DDR I/O input logic.

- Bit 3 ENFORCERST
 *0: No DDR I/O ping-pang counter reset every horizontal line.
 1: DDR I/O ping-pang counter reset every horizontal line.
- Bit 2 EN_FLAG_PWDN
 *0: No Active/Precharge power-down mode supported.
 1: Active/Precharge power-down mode supported.
- Bit 1 REG_RC_EXT
 *0: Kill definition in 3D5.1B<7:4>.
 1: REG_RC = 3D5.1B<7:4> + 7 cycles
- Bit 0 NOGRHX

9.47. Bias Control

Address: 3X4H/3X5H Index: 60 Access: Read/Write

- Bits 7:6 DDR I/O Control
 00: Bias power-down mode, work at maximum driving strength.
 01: Debugging stages.
 10: Debugging stages.
 *11: Normal work mode, driving strength control.
- Bit 5 BIAS_ONOFF
 0: Disable driving strength control and temperature tracking.
 *1: Control driving strength and temperature vibration.
- Bits 4:3 SYNC_MODE
 *00: Pure asynchronous mode with 2 cycle synchronization.
 01: Asynchronous mode with 1 cycle synchronization.
 10: Synchronous mode (no synchronization cycles).
 11: Reserved.
- Bits 2:0 Maximum physical memory size.
 *000: 0 – 128MB
 001: 0 – 64MB
 010: 0 – 32MB
 011: 0 – 16MB
 100: 0 – 8MB
 101: Reserved
 110: Reserved
 111: Reserved

9.48. Misc. Internal Register 5

Address: 3X5H Index: 61 Access: Reserved

- Reserved
- Bit 7
- Bit 6 SEL25DDR
 *1: DDR I/O perform 2.5v signaling
 0: DDR I/O perform 1.8v signaling.

- Bit 5 PW_ONDEMAND_SCHEM
- *0: application power on demand (GE+DVD).
 - 1: application power on demand (GE+DVD+WIN1+WIN2).
- Bit 4 EN_PW_ONDEMAND
- *0: disable power on demand.
 - 1: enable power on demand.
- Bit 3:2 MCK2_FQ_H
- *0: MCK2 is not divided from the PLL output.
 - 1: MCK2 is divided by2 from the PLL output.
 - 2: MCK2 is divided by3 from the PLL output.
 - 3: MCK2 is divided by4 from the PLL output.
- Bit 1:0 MCK_FQ_H
- *0: MCK is not divided from the PLL output.
 - 1: MCK is divided by2 from the PLL output.
 - 2: MCK is divided by3 from the PLL output.
 - 3: MCK is divided by4 from the PLL output.

10. Memory Interface Register Description

10.1. Manually initialize memory power-up process

Address: 3X4H/3X5H Index: 1A Access: Read/Write

- Bit 7 Reserved
- Bit 6 REG_REFR
1: Manually starts memory automatic refresh.
0: Manually stops memory automatic refresh.
- Bit 5 REG_MRS
1: Manually loads in memory mode register.
0: Manually stops loading in memory mode register.
- Bit 4 REG_ENDLL
1: Manually enables DLL inside DDR memory.
0: Manually disables DLL inside DDR memory
- Bit 3 REG_RSTDLL
1: Manually resets DLL inside DDR memory.
0: Manually stops resetting DLL inside DDR memory.
- Bit 2 REG_PWDN
1: Manually starts memory power down.
0: Manually stops memory power down.
- Bit 1 REG_PALL
1: Manually starts pre-charging all memory banks.
0: Manually stops pre-charging all memory banks.
- Bit 0 Reserved

10.2. Memory Timing Control 1

Address: 3X4H/3X5H Index: 1B Access: Read/Write

- Bits 7:5 REG_RFC (tRFC: Row refresh cycle time)
*Default value is 1H (0H ~ 7H)
 $\text{Cycles (tRFC)} = \text{tRC} + \text{REG_RFC} * 2 (\text{tCK})$
- Bits 4:0 REG_RC (tRC: Row cycle time)
*Default value is 05H (00H ~ 1FH)
 $\text{Cycles (tRC)} = \text{REG_RC} + 9 (\text{tCK})$

10.3. Memory Timing Control 2

Address: 3X4H/3X5H Index: 1C Access: Read/Write

- Bits 7:5 REG_RRD (tRRD: Row active to Row)
*Default value is 0H (0H ~ 7H)
 $\text{Cycles (tRRD)} = \text{REG_RRD} + 2 (\text{tCK})$

Bits 4:0 REG_RAS (tRAS: Row active time)
 *Default value is 03H (00H ~ 1FH)
 Cycles (tRAS) = REG_RAS + 6 (tCK)

10.4. Memory Timing Control 3

Address: 3X4H/3X5H Index: 1D Access: Read/Write

Bits 7:4 REG_RCDR (tRCDR: RAS to CAS delay for Read)
 *Default value is 4H (0H ~ FH) Cycles (tRCDR) = REG_RCDR + 1 (tCK)

Bits 3:0 REG_RCDW (tRCDW: RAS to CAS delay for Write) *Default value is 4H (0H ~ FH)
 Cycles (tRCDW) = REG_RCDW + 1 (tCK)

10.5. CRT Module Testing Register

Address: 3X4H/3X5H Index: 1E Access: Read/Write

Bit 7 ENWRAP

1: Enable access to extended memory above 256KB.
 *0: Disable access to extended memory above 256KB.

Bit 6 PROT3C2

1: Protect VGA miscellaneous output register 3C2H.
 *0: Enable writing to 3C2H

Bits 5:3 Reserved

Bit 2 INTERLACE

1: Interlace mode.
 *0: Non-interlace mode.

<1:0>: Reserved

Reserved

Bits 1:0

10.6. Memory Timing Check 4

Address: 3X4H/3X5H Index: 20 Access: Read/Write

Bits 7:6 REG_BA0_SEL
 Select what will the real BA0 on the memory bus. This is only effective when ONLY2BANK(3D4.5F[1]) is high.
 *0: normally as is (BA0); 1: fixed as low (1'b0);
 2: fixed as high (1'b1); 3: reserved

Bit 5 Reserved

Bit 4 UNCHN16 (not effective in column132 mode)
 0: Disable 16-bit planar mode.
 1: Enable 16-bit planar mode.

Bits 3:2 Reserved

- Bit 1 VM_SWITCH
 *0: The 1st memory port is treated as virtual frame-buffer.
 1: The 2nd memory port is treated as virtual frame-buffer.
- Bit 0 VM_ENABLE
 *0: Disable Virtual Frame-buffer on system side.
 1: Enable Virtual Frame-buffer on system side (Frame-Buffer-less).

10.7. Linear Addressing

Address: 3X4H/3X5H Index: 21 Access: Read/Write

- Bit 7 NEW132
 0: 80-column text mode *
 1: 132-column text mode
- Bit 6 REG_ADR17
 ROM address bit17
- Bit 5 ENLINEAR
 0: Disable linear addressing *
 1: Enable linear addressing
- Bit 4 REG_ADR16
 ROM address bit16
- Bit 3 MEM_SIZE_FIX_1
 Power-up configuration from PD<14>. This bit is used to be boot-up configurable to set actual existing memory size. It is for a fix in Rev. B.
 0: Blocking PCI base address bit24 (maximim 32MB) *
 1: No blocking PCI base address bit24 (maximim 16MB)
- Bit 2 EN256BIOS
 0: Disable 256K BIOS support *
 1: Enable 256K BIOS support
- Bit 1 SIG_EN
 0: MCM signature disabled *
 1: MCM signature enabled
- Bit 0 MCM_LOAD
 0: MCM BIST random number generator seed load disabled *
 1: MCM BIST random number generator seed load enabled

10.8. CPU Latch Read Back Register

Address: 3X4H/3X5H Index: 22 Access: Read/Write

- Bits 7:0 Latched data pointed by VGA read map select register

10.9. Memory Timing Check 5

Address: 3X4H/3X5H Index: 23 Access: Read/Write

- Bits 7:6 REG_XSRDD (Cycles delay from SELF REFRESH to READ command for DDR memory)
 0: 100 CLK; 1: 200 CLK (※); 2: 300 CLK; 3: 400 CLK

- Bit 5 **DISABLE_H_QUEUE**
 0: Enable high priority arbitration queue(for read only clients) -- (✖)
 1: Disable high priority arbitration queue.
- Bit 4 **INIT_MEM**
 0: Initialization finished, normal operation must be in this status. (✖)
 1: Manually initialize memory controller and arbitration circuit.
- Bit 3 **MEM_DLL_OFF**
 This bit is mapped to A0 of EMR (extended mode register) of DDR memory.
 0: Turn on DLL circuit on the DDR memory side. (✖)
 1: Turn off DLL circuit on the DDR memory side.
(any change of this bit can take effect only if be followed by a manual memory initialization done by set on bit4 of this register or by following the process described in register 3X5.1A)
- Bits 2:1 **MEM_DRV_STRENGTH**
 This definition depends on an individual DDR memory chip specification released by memory vendor. These two bits are mapped to A6 & A1 of EMR (extended mode register) accordingly.
 0: normal impedance(full driving strength);
 1: weak impedance(60% of full driving strength); (✖)
 2: matched impedance(30% of full driving strength);
 3: Reserved.
(any change of this bit can take effect only if be followed by a manual memory initialization done by set on bit4 of this register or by following the process described in register 3X5.1A)
- Bit 0 **CLSMEM**
 Close access to external memory, default value is 0H.

10.10. Memory Timing Check 6

Address: 3X4H/3X5H Index: 26 Access: Read/Write

- Bits 7:2 **DPA_EXT_CCODE**
 Coarse code input to select coarse delay range. Needs to set SEL_EXT_DELYCTRL to 1.
 *default value is 00000H
- Bits 1:0 **C_RNG_SEL**
 Limit coarse delay line working range; Needs to set SEL_EXT_DELYCTL to 0, set SEL_CTL_NEW to 1.
 *default value is 0H

10.11. Memory Misc. Setting (protected by 3C5.0EH_new bit 7)

Address: 3X4H/3X5H Index: 2A Access: Read/Write

- Bit 7 **MI_MODE**
 1: External dual ports. 0: External single port (✖).
- Bit 6 **EN32**
 1: Internal 32-bit data path. 0: Internal 8/16 bits data path (✖).
- Bit 5 **Reserved**

- Bit 4 ENCONF
1: Power down using ROMCS# (✖). 0: Don't power down using ROMCS#.
- Bit 3 Reserved
- Bit 2 RST_CLKSEL
1: Substitute internal MCK with PCICLK.
0: Normal (✖).
- Bits 1:0 MEM_SIZE (The switch point in one linear logic memory space when two ports of physical memory consists of this logic memory space)
0: 32M (✖); 1: 64M; 2: 128M; 3: 256M

10.12. Memory Controller 0

Address: 3X4H/3X5H Index: 2C Access: Read/Write

- Bits 7:6 REG_FIFO_LEVEL<3:2> (FIFO full water marker for High Priority Queue in Memory Controller.)
0: 8 levels; 1: 16 levels; 2: 32 levels (✖); 3: 32 levels;
- Bits 5:4 REG_FIFO_LEVEL<1:0> (FIFO full water marker for Low Priority Queue in Memory Controller.)
0: 8 levels; 1: 16 levels; 2: 32 levels (✖); 3: 32 levels;
- Bit 3 EN_PREDETECT (Enable predicting mechanism in Memory Controller.)
*Default value is 0.
- Bits 2:0 MEM_TYPE (SDR/DDR SDRAM types supported)
0: Reserved; 1: *1: 4Mx32/4Mx16 (4 banks);
2: 8Mx32/8Mx16 (2 banks); 3: 16Mx16 (4 banks); (✖)
4: 32M x 32 (4 banks); 5~7: Reserved

10.1. DPA Control Register 1

Address: 3D4/3D5H Index: 2E Access: Read/Write

- Bit 7 REG_DPAOFF
0: Turn on memory clock DPA *
1: Turn off memory clock DPA
- Bit 6 Reset DPA
0: Normal condition *
1: Reset DPA (bypass DPA in the other word)
- Bit 5 Adjust half more clock on internal DQM output control between two concatenated Read to Write command sequence.
0: Give half more clock control *
1: Normal condition
- Bit 4 DDR I/O input power-on enable look ahead cycles. Input I/O logic enable look ahead cycles are one cycle less.
1: 3 cycles
*0: 2 cycles

- Bit 3 DDR I/O output enable look ahead cycles
 1: 2 cycles
 *0: 1 cycle
- Bit 2 REG_DLLOFF
 0: Turn on DLL circuit especially for DDR memory interface *
 1: Turn off DLL circuit especially for DDR memory interface
- Bit 1 REG_DLLRST
 0: Normal DLL functioning *
 1: Reset DLL circuit especially for DDR memory interface
- Bit 0 REG_DQSMUX
 0: Select to have 2 DQS working in each memory I/O bar *
 1: Select to have 8 DQS working in each memory I/O bar
 Default value is 04H.

10.2. Performance Tuning Register

Address: 3D4/3D5H Index: 2F Access: Read/Write

- Bit 7 RCT16
 0: Normal condition *
 1: Only fetch 16 FIFO entries one time at the beginning of one horizontal line
- Bit 6 REF12
 To define refresh cycles together with 3X5.5D.bit7 & 3X5.11.bit6 for each horizontal line.
- | REG_QT | REF12 | 3D5.11.6 | refresh cycles per horizontal line |
|--------|-------|----------|------------------------------------|
| 0 | 0 | 0 | 3 |
| 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 0 | 7 |
| 1 | 0 | 1 | 9 |
| 1 | 1 | 0 | 11 |
| 1 | 1 | 1 | 13 |
- Bit 5 BLNKSEL
 0: Normal blank *
 1: Blank is the inverse of display enable
- Bit 4 RCT8
 0: Normal condition *
 1: Only fetch 8 FIFO entries one time at the beginning of one horizontal line
- | RCT16 | RCT8 | |
|-------|------|--------------------------|
| 0 | 0 | Fetch 32 entries at most |
| 1 | 0 | Fetch 16 entries at most |
| 0 | 1 | Fetch 8 entries at most |
| 1 | 1 | Fetch 64 entries at most |
- Bits 3:2 Memory read ready control.
 0: Normal speed *
 1: 1 clock delay
 2: 2 clocks delay
 3: 3 clocks delay

- Bit 1 WBUFLE1
 0: Select LCLKI as the source for internal LCLK *
 1: Select VCLKI as the source for internal LCLK
- Bit 0 SET_CTL_NEW
 0: Original control logic would be effective
 1: Select new fine-coarse search logic control. (Needs to set SEL_EXT_DELYCTRL to 0) *

10.13. Memory Mapping Control 0 (REG_MAP)

Address: 3X4H/3X5H Index: 31 Access: Read/Write

- Bits 7:4 Mapping control on the 1st memory bank, which bit is used as CS0/CS1;
 *0: Bank[1:0] mapped to two continuous address bits (i.e. AD[9:8] or AD[10:9] or AD[11:10]);
 1: Bank[1] is one bit left shift;
 2: Bank[1] is two bits left shift;
 3: Bank[1] is three bits left shift;
 4~5: Reserved
- Bits 3:0 Reserved

10.3. MCK Clock Duty Adjustment Control

Address: 3CEH/3CFH Index: 3C Type: Read/Write

- Bits 7:5 Reserved
- Bits 4:0 MCK clock duty adjustment
 For HIGH time:
 10000 ~ 11111: Bypass to 16 steps
 For LOW time:
 01111 ~ 00000: Bypass to 16 steps
 * The default value is 10H.

10.14. Memory Controller 1

Address: 3D4/3D5H Index: 5D Access: Read/Write

- Bit 7 To define refresh cycles together with 3X5.2F.bit6 & 3X5.11.bit6 for each horizontal line.
 Default value is 0.
- Bit 6 This register bit only takes effect when REG_DDR is set and MI_MODE and REG64 are not set.
 0: Not single 128-bit external DDR memory bus *
 1: Single 128-bit external DDR memory bus
- Bits 5:1 REG_PIPE_ADJUST
 *Default 01100b
- Bit 0 REG64:
 0: 128-bit external memory bus *
 1: 64-bit external memory bus

10.15. Memory Timing Control 1

Address: 3D4/3D5H Index: 60 Access: Read/Write

- Bits 7:6 DDR I/O control
- 00: Bias power down mode, work at maximum driving strength
 - 01~10: debugging stages
 - *11: Normal work mode, driving strength control.
- Bit 5 Reserved
- Bits 4:3 SYNC_MODE
- *00: Pure asynchronous mode with 2 cycle synchronization.
 - 01: Asynchronous mode with 1 cycle synchronization.
 - 10: Synchronous mode (no synchronization cycles).
 - 11: Reserved.
- Bits 2: 0 Maximum physical memory size.
- | | |
|------------------|---------------------|
| *000: 0 ~ 256 MB | 001: 0 ~ 128 MB |
| 010: 0 ~ 64 MB | 011: 0 ~ 32MB |
| 100: 0 ~ 16 MB | 101 ~ 111: Reserved |

10.16. Memory Timing Control 2

Address: 3D4/3D5H Index: 61 Access: Read/Write

- Bit 7 Reserved
- Bit 6 *1: DDR I/O perform 2.5v signaling
- 0: DDR I/O perform 1.8v signaling.
- Bit 5 PW_ONDEMAND_SCHEM
- *0: application power on demand (GE+DVD).
 - 1: application power on demand (GE+DVD+WIN1+WIN2).
- Bit 4 EN_PW_ONDEMAND
- *0: disable power on demand.
 - 1: enable power on demand
- Bits 3:2 MCK2_FQ_H
- *0: MCK2 is not divided from the PLL output.
 - 1: MCK2 is divided by2 from the PLL output.
 - 2: MCK2 is divided by3 from the PLL output.
 - 3: MCK2 is divided by4 from the PLL output.
- Bits1: 0 MCK_FQ_H
- *0: MCK is not divided from the PLL output.
 - 1: MCK is divided by2 from the PLL output.
 - 2: MCK is divided by3 from the PLL output.
 - 3: MCK is divided by4 from the PLL output.

10.17. Memory Timing Control 3

Address: 3D4/3D5H Index: 62 Access: Read/Write

- Bit 7 VREF_SEL_INT
*0: DDR I/O Vref is provided from outside.
1: DDR I/O Vref is generated inside.
- Bit 6 ENGERTY
1: Two cycles PCI write bursting.
*0: Normal PCI write bursting.
- Bit 5 ENSHRT
1: Enable short command.
*0: Normal condition.
- Bit 4 DINALLTIMEON
*0: Memory I/O input buffer dynamically on.
1: Memory I/O input buffer always on.
- Bits 3:2 FIFO_L_BURST
*0: Allow 64 bursting Low Priority R/W when High Priority command is ready ;
1: Allow 32 bursting Low Priority R/W when High Priority command is ready ;
2: Allow 16 bursting Low Priority R/W when High Priority command is ready ;
3: Allow 8 bursting Low Priority R/W when High Priority command is ready ;
- Bits 1:0 TMRCTEST
Memory refresh cycle test.
*0: normal; 1: every other scan;
2: every fourth scan; 3: No refresh;

10.4. Enhancement Register 1

Address: 3X4H/3X5H Index: 63 Access: Read/Write

- Bits 7:6 MCK_FQ
*0: MCK is not divided from the PLL output.
1: MCK is divided by2 from the PLL output.
2: MCK is divided by3 from the PLL output.
3: MCK is divided by4 from the PLL output

Bits 5:4 FOLD7,FOLD6

16 MUX81P are put into the chip for debugging purpose. A,B,C are used to select which signal will be presented outside through PINCAPD,15:8> and PINDPX<7:0>.

C(ASYMN,GR0F.bit5)	B(FOLD7)	A(FOLD6)	Input of MUX81P
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4*
1	0	1	D5
1	1	0	D6
1	1	1	D7

Bits 3:2 MCK2_FQ

- *0: MCK2 is not divided from the PLL output.
- 1: MCK2 is divided by2 from the PLL output.
- 2: MCK2 is divided by3 from the PLL output.
- 3: MCK2 is divided by4 from the PLL output

Bits 1:0 Reserved

10.5. DPA Control Register 2

Address: 3X5H Index: 64 Access: Read/Write

Bits 7:4 Delay Control2 on DPA input CLKREF.

Bits 3:0 Delay Control1 on DPA input CLKREF.

10.18. Memory Timing Control 4

Address: 3D4/3D5H Index: 80 Access: Read/Write

Bit 7 Reserved

Bits 6:4 REG_AL (tAL: Additive Latency)

- *Only applied for DDRII, default value is 0H (0H ~ 7H)
- Cycles (tAL) = REG_AL (tCK)

Bit 3 Reserved

Bits 2:0 REG_CL (tCL: Read Latency)

- *Default value is 1H (0H ~ 7H)
- Cycles (tCL) = REG_RFC + 2 (tCK)

10.19. Memory Timing Control 5

Address: 3CE/3CFH Index: 81 Access: Read/Write

Bit 7 Reserved

Bits 6:3 REG_WL (tWL: Write Latency)

- *Only applied for DDRII, default value is 0H (0H ~ 7H)
- Cycles (tWL) = REG_WL + 1 (tCK)

Bits 2:0 REG_RSC (tRSC: Mode register set cycle time)
 *Default value is 0H (0H ~ 7H)
 $\text{Cycles (tRSC)} = \text{REG_RSC} + 2 (\text{tCK})$

10.20. Memory Timing Control 6

Address: 3CE/3CFH Index: 82 Access: Read/Write

Bit 7 REG_CCD (tCCD)
 Column address to Column address cycle time.
 1: 2 cycles
 *0: 1 cycle

Bits 6:4 Reserved

Bits 3:0 REG_RP (tRP: Row precharge time)
 *Default value is 0H (0H ~ FH)
 $\text{Cycles (tRP)} = \text{REG_RP} + 2 (\text{tCK})$

10.21. Memory Timing Control 7

Address: 3CE/3CFH Index: 83 Access: Read/Write

Bit 7 Reserved

Bits 6:4 REG_WL (tWL: Write Latency)
 *Only applied for DDRII, default value is 0H (0H ~ 7H)
 $\text{Cycles (tWL)} = \text{REG_WL} + 1 (\text{tCK})$

Bit 3 Reserved

Bits 2:0 REG_W2P (tW2P: Last data in to Row precharge)
 *Default value is 1H (0H ~ 7H)
 $\text{Cycles (tW2P)} = \text{REG_W2P} + 2 (\text{tCK})$

10.22. Memory Timing Control 8

Address: 3CE/3CFH Index: 84 Access: Read/Write

Bit 7 Reserved

Bits 6:5 REG_R2W (Last read strobe to next write strobe turn around time)
 *Default value is 1H (0H ~ 4H)
 $\text{Cycles} = \text{REG_R2W} + 1 (\text{tCK})$

Bit 4 Reserved

Bits 3:2 REG_R2P (Last read strobe to next precharge turn around time)
 *Default value is 0H (0H ~ 4H)
 $\text{Cycles} = \text{REG_R2P} + 0 (\text{tCK})$

Bits 1:0 REG_PWDNEX (tPWDNEX: power down exit time)
 *Default value is 0H (0H ~ 4H)
 $\text{Cycles (tPWDNEX)} = \text{REG_PWDNEX} + 2 (\text{tCK})$

10.23. I/O Pads Driving Strength Control 1

Address: 3CEH/3CFH Index: 94-90 Access: Read Only

- Bits 39:35 Software coarse delay code for $\frac{1}{4}$ cycle (Default value is 5'b00000).
- Bit 34 FORCE_UPDATE4.
1: Force to update delay code for $\frac{1}{4}$ cycle
*0: Automatically update delay code for $\frac{1}{4}$ cycle
- Bit 33 SEL_SWCODE4.
1: Select software delay code for $\frac{1}{4}$ cycle instead of the code from DLL
*0: Select delay code for $\frac{1}{4}$ cycle from DLL
- Bit 32 Reserved
- Bits 31:24 REFPSEL, REFNSSEL (memory data pins).
* Default value is 44H.
- Bits 23:16 MDPSEL, MDNSSEL (memory I/O slew rate control).
* Default value is 44H.
- Bits 15:8 MCPSEL, MCNSSEL (memory command/clock pins).
* Default value is 44H.
- Bits 7:0 CLKPSEL, CLKNSSEL (memory clock pins, reserved).
* Default value is 44H.

11. Hardware Cursor Register Descriptions

The Volari XP10 supports the Windows® compatible hardware cursor. The hardware cursor operates only in the extended planar and packed pixel modes. The cursor size can be selected between 32x32, 64x64 and 128x128. Two 2-bits-per-pixel images define the cursor shape, and Table 11-1 shows how these two bits operate on each pixel. The hardware cursor pattern is stored in the off-screen area.

Table 11-1 Cursor Pixel Operation

Plane 0 (AND)	Plane 1 (XOR)	Pixel Operation (Windows®)	Pixel Operation (X11)
1	0	Transparent	Cursor Background Color
1	1	VGA Data Inversion	Cursor Foreground Color
0	1	Cursor Foreground Color	Transparent
0	0	Cursor Background Color	Transparent

In the register descriptions that follow, all of the reserved bits are read back as 0 unless otherwise specified.

11.1. Hardware Cursor1 Position

Address: 3D4H/3D5H Index: 43-40 Access: Read/Write

- Bits 31:28 Reserved
- Bits 27:16 Hardware cursor1 position in the Y-dimension
- Bits 15:12 Reserved
- Bits 11:0 Hardware cursor1 position in the X-dimension
Note: This register setting cannot take effect until Write 3D5.43.

11.2. Hardware Cursor Pattern Location 0

Address: 3D4H/3D5H Index: 44 Access: Read/Write

- Bits 7:0 Hardware Cursor Mask Map Storage Location, which is 1KB aligned in the frame buffer.

11.3. Hardware Cursor Pattern Location 1

Address: 3D4H/3D5H Index: 45 Access: Read/Write

- Bits 7:0 Hardware Cursor Mask Map Storage Location, which is 1KB aligned in the frame buffer.

11.4. Hardware Cursor1 X-offset & Y-offset

Address: 3D4H/3D5H Index: 47-46 Access: Read/Write

- Bit 15 Reserved
- Bits 14:8 Hardware cursor1 Y-offset
- Bit 7 Reserved

Bits 6:0 Hardware cursor1 X-offset
Note: This register setting cannot take effect until Write 3D5.43.

11.5. Hardware Cursor1 Color

Address: 3D4H/3D5H Index: 4F-48 Access: Read/Write

Bits 31:28 Reserved
Bits 27:16 Hardware cursor1 background color
Bits 15:12 Reserved
Bits 11:0 Hardware cursor1 foreground color

11.6. Hardware Cursor1 Control

Address: 3D4H/3D5H Index: 50 Access: Read/Write

Bit 7 HCEN
 0: Turn off Hardware Cursor1 *
 1: Turn on Hardware Cursor1
Bit 6 HCX11
 0: MS Windows cursor mode*
 1: X11 compatible cursor mode
Bit 5 HCSEL4C
 Replace VGA data inversion (11 for combination of Plane0 and Plane1)
 0: Disable cursor color3 control *
 1: Enable cursor color3 control (defined in 3d5.74, 3d5.75, and 3d5.76)
Bit 4 HCSEL3C
 Replace VGA data inversion (11 for combination of Plane0 and Plane1)
 0: Disable cursor color3 control 2 *
 1: Enable cursor color3 control 2 (defined in 3d5.70, 3d5.71, and 3d5.72)
Bit 3 VHCEN
 0: Turn off Video Hardware Cursor1 (WIN2)*
 1: Turn on Hardware Cursor1 (WIN2)
Bit 2 ENOLDHC
 0: Disable old circuit for Hardware Cursor *
 1: Enable old circuit for Hardware Cursor
Bits 1:0 Cursor size.
 0: 32 x 32 *
 1: 64 x 64
 2: 128 x 128
 3: Reserved

11.7. Hardware Cursor2 Control

Address: 3X5H Index: 65 Access: Read/Write

Bit 7	HC2EN 0: Turn off Hardware Cursor2 * 1: Turn on Hardware Cursor2
Bit 6	HC2X11 0: MS Windows cursor mode * 1: X11 compatible cursor mode
Bit 5	HC2SEL4C/HC2APREMUTI Replace VGA data inversion (11 for combination of Plane0 and Plane1) 0: Disable cursor color3 control * 1: Enable cursor color3 control (defined in 3d5.7d, 3d5.7e, and 3d5.7f) <i>If both HC2EN and HC2AEN are high, this bit is to control whether alpha cursor pattern is pre-multiplied.</i> 1: <i>pre-multiplied</i> *0: <i>not pre-multiplied</i>
Bit 4	HC2SEL3C Replace VGA data inversion (11 for combination of Plane0 and Plane1) 0: Disable cursor color control 2 * 1: Enable cursor color control 2 (defined in 3d5.7a, 3d5.7b, and 3d5.7c) <i>If both HC2EN and HC2AEN are high, this bit is to control alpha cursor pattern color format.</i> 1: <i>8888color</i> *0: <i>8332color</i>
Bit 3	Configure HC2 as alpha cursor.
Bit 2	HC2ONTOP 0: The first Hardware Cursor on top if two hardware cursors overlay * 1: Enable the second Hardware Cursor on top if two hardware cursors overlay
Bits 1:0	Cursor size (HC2_128, HC2_64). 0: 32 x 32 * 1: 64 x 64 2: 128 x 128 3: Reserved

11.8. Hardware Cursor2 Position

Address: 3D4H/3D5H Index: 69-66 Access: Read/Write

Bits 31:28	Reserved
Bits 27:16	Hardware cursor2 position in the Y-dimension
Bits 15:12	Reserved
Bits 11:0	Hardware cursor2 position in the X-dimension

11.9. Hardware Cursor2 Color

Address: 3D4H/3D5H Index: 6F-6A Access: Read/Write

Bits 47:24	Hardware cursor2 background color
Bits 23:0	Hardware cursor2 foreground color

11.10. Hardware Cursor1 Color2

Address: 3D4/3D5H Index: 72 – 70 Access: Read/Write

Bits 23:0 Hardware Cursor1 Color2.

11.11. Hardware Cursor2 X-offset

Address: 3D4H/3D5H Index: 73 Access: Read/Write

Bit 7 Reserved

Bits 23:0 Hardware cursor2 X-offset

11.12. Hardware Cursor1 Color3

Address: 3D4/3D5H Index: 76 – 74 Access: Read/Write

Bits 23:0 Hardware Cursor1 Color3.

11.13. Hardware Cursor2 Y-offset

Address: 3D4H/3D5H Index: 77 Access: Read/Write

Bit 7 Reserved

Bits 23:0 Hardware cursor2 Y-offset

11.14. Hardware Cursor2 Pattern Location

Address: 3D4H/3D5H Index: 79 - 78 Access: Read/Write

Bits 15:0 Hardware cursor2 map storage location, which is 1KB alignment in the frame buffer for 32 x 32, 64 x 64, and 4KB alignment for 128 x 128.

11.15. Hardware Cursor2 Color3 & Color2

Address: 3D4H/3D5H Index: 7F-7A Access: Read/Write

Bits 47:24 Hardware cursor2 color3

Bits 23:0 Hardware cursor2 color2

12. SYNDAC Register Descriptions

In the register descriptions that follow all of the reserved bits are read back as 0 unless otherwise specified.

12.1. DAC Pixel Mask Register

Address: 3C6H Access: Read/Write

Bits 7:0 Palette address mask

12.2. SYNDAC Command Register

Address: 3C6H Access: Read/Write

Bits 7:4 Color mode select:
0000: Pseudo color mode
0001: Hi-Color mode, 15-bit direct interface
0010: Multiplexed pseudo color mode (16 bit pixel bus)
0011: XGA color mode, 16-bit direct interface
1101: True Color mode, 24-bit direct interface
All other codes are reserved

Bit 2 DAC Enable:
1: DAC is off
0: DAC is on (default).
DAC is on only if this bit and 3C5.20.0 are on

Bit 0 RAMDAC™
1 = RAMDAC™
0 = Bypass RAMDAC™
Reset: 00h
This register is enabled after four successive access to Pixel Mask Register (read 3C6 four times).

12.3. DAC Read Data Address Register

Address: 3C7H Access: Write Only

Bits 7:0 Read data address
Reset: N/A

12.4. DAC Write Data Address Register

Address: 3C8H Access: Read/Write

Bits 7:0 Write data address
Reset: N/A

12.5. DAC Palette Data Register

Address: 3C9H Access: Read/Write

Bits 7:0 Palette data

12.6. MCLK Frequency Control Register 0

Address: 3C5H Index: 16 Access: Read/Write

Bits 7:0 Numerator of MCLK frequency generator
Reset: 00h

12.7. MCLK Frequency Control Register 1

Address: 3C5H Index: 17 Access: Read/Write

Bits 7:6 K factor of MCLK frequency generator
Bits 5:0 Denominator of MCLK frequency generator
Reset: 00h

12.8. VCLK-1 Frequency Control Register 0

Address: 3C5H Index: 18 Access: Read/Write

Bits 7:0 Numerator of VCLK-1 frequency generator (This is the Low HEX in the adjustment table of VCLK.)
Reset: 00h

12.9. VCLK-1 Frequency Control Register 1

Address: 3C5H Index: 19 Access: Read/Write

Bits 7:6 K factor of VCLK-1 frequency generator
Bits 5:0 Denominator of VCLK-1 frequency generator (This is the High HEX in the adjustment table of VCLK.)
Reset: 00h

12.10. VCLK-2 Frequency Control Register 0

Address: 3C5H Index: 1A Access: Read/Write

Bits 7:0 Numerator of VCLK-2 frequency generator (This is the Low HEX in the adjustment table of VCLK.)
Reset: 00h

12.11. VCLK-2 Frequency Control Register 1

Address: 3C5H Index: 1B Access: Read/Write

Bits 7:6 K factor of VCLK-2 frequency generator
Bits 5:0 Denominator of VCLK-2 frequency generator (This is the High HEX in the adjustment table of VCLK.)
Reset: 00h

12.12. MCLK and VCLK Frequency Tables

In general, MCLK or VCLK frequency can be derived from the following equation:

$$\text{Frequency} = \text{OSC} \times (N+7) / [(M+1) \times 2^K]$$

And: Error = (Freq. Out – Freq. Expected) * (100) / (Freq. Out)

Table 6-1. Clock Frequency OSC=14.31818MHz

Register Values		N	M	K	Freq. Out	Freq. Exp.	Error
Hi(hex)	Low(hex)				MHz	MHz	
88	3E	62	8	2	25.057	25.175	-0.0047
89	4F	79	9	2	28.311	28.322	-0.0004
88	5D	93	8	2	36.153	36.000	0.0043
83	30	48	3	2	40.091	40.000	0.0023
85	4A	74	5	2	41.932	42.000	-0.0016
84	42	66	4	2	44.148	44.000	0.0034
84	43	67	4	2	44.744	44.900	-0.0035
84	48	72	4	2	47.727	48.000	-0.0057
43	1B	27	3	1	50.114	50.350	-0.0047
46	33	51	6	1	52.798	52.800	0.0000
42	18	24	2	1	57.273	57.270	0.0000
43	21	33	3	1	58.705	58.800	-0.0016
43	23	35	3	1	61.568	61.600	-0.0005
4A	63	99	10	1	63.835	64.000	-0.0026
48	53	83	8	1	65.148	65.000	0.0023
46	43	67	6	1	67.116	67.200	-0.0012
44	33	51	4	1	70.398	70.400	0.0000
44	34	52	4	1	71.591	72.000	-0.0057
42	22	34	2	1	75.170	75.000	0.0023
44	39	57	4	1	77.557	77.000	0.0072
44	3B	59	4	1	79.943	80.000	-0.0007
44	42	66	4	1	88.295	88.000	0.0034
44	44	68	4	1	90.682	90.000	0.0076
44	4A	74	4	1	97.841	98.000	-0.0016
04	22	34	4	0	100.227	100.000	0.0023
07	3C	60	7	0	108.182	108.000	0.0017
02	19	25	2	0	118.125	118.000	0.0011
03	22	34	3	0	120.273	120.000	0.0023
05	3A	58	5	0	135.000	135.000	0.0000
05	4B	75	5	0	169.773	170.000	-0.0013
05	5A	90	5	0	200.455	200.000	0.0023

Table 6-2. Clock Frequency OSC=17.734475 MHz

Register Values		N	M	K	Freq. Out	Freq. Exp.	Error
Hi(hex)	Low(hex)				MHz	MHz	
88	31	49	8	2	25.272	25.175	0.0039
88	38	56	8	2	28.376	28.322	0.0019
88	49	73	8	2	35.913	36.000	-0.0024
86	40	64	6	2	39.903	40.000	-0.0024
84	31	49	4	2	42.120	42.000	0.0029
85	3D	61	5	2	43.704	44.000	-0.0067
85	3F	63	5	2	44.971	44.900	0.0016
84	39	57	4	2	48.032	48.000	0.0007
44	1A	26	4	1	50.249	50.350	-0.0020
46	28	40	6	1	53.205	52.800	0.0077
47	32	50	7	1	57.146	57.270	-0.0022
43	19	25	3	1	58.525	58.800	-0.0047
45	29	41	5	1	62.072	61.600	0.0077
48	40	64	8	1	63.846	64.000	-0.0024
47	3A	58	7	1	65.028	65.000	0.0004
46	35	53	6	1	67.614	67.200	0.0062
45	30	48	5	1	70.940	70.400	0.0077
44	29	41	4	1	72.417	72.000	0.0058
44	2B	43	4	1	75.373	75.000	0.0050
44	2C	44	4	1	76.851	77.000	-0.0019
46	40	64	6	1	79.807	80.000	-0.0024
45	3D	61	5	1	87.408	88.000	-0.0067
44	35	53	4	1	90.152	90.000	0.0017
44	3A	58	4	1	97.542	98.000	-0.0047
04	1A	26	4	0	100.498	100.000	0.0050
09	3B	59	9	0	108.022	108.000	0.0002
04	20	32	4	0	118.233	118.000	0.0020
03	1A	26	3	0	120.597	120.000	0.0050
06	35	53	6	0	135.228	135.000	0.0017
05	3B	59	5	0	169.748	170.000	-0.0015
05	47	71	5	0	200.151	200.000	0.0008

12.13. SYNDAC Setup Register

Address: 3C5H Index: 20 Access: Read/Write

- Bit 7 Reserved
- Bit 6 Multiplex Mode Sync Mechanism Enable:
 - 1: Enable synchronization in multiplexed mode for high VCLK tracking;
 - 0: normal mode
- Bit 5 Enable simultaneous VAFC and Playback display:
 - 0: support simultaneous VAFC and Playback display
 - 1: playback only
- Bit 4 During simultaneous VAFC and Playback display:
 - 0: VAFC is on top
 - 1: Playback is on top
- Bit 3 Enable DAC test mode (active high)
- Bit 2 Enable VIDEO mode (active high)
- Bits 1:0 Select VIDEO mode:
 - x0: Hi-color (5-5-5)
 - x1: XGA Color (5-6-5)
 - 0x: Video playback , True Color
 - 1x: Video playback, 256 color

Others are reserved.
Reset: 00h

12.14. Signature Control Register

Address: 3C5H Index: 21 Access: Read/Write

- Bit 7 When write:
 - 1: Enable signature generator.
 - 0: Disable signature generator.

When read:

 - 1: busy
 - 0: completed
- Bit 6 Signature enable source select:
 - 0: CRT
 - 1: LCD
- Bits 5:0 Select which 16 bits of 48 bits signature generator output to register 3C5.23-22
 - 00h: bit 15~bit 0
 - 01h: bit31 ~ bit 16
 - 02h: bit 47 ~ bit 32
 - others: bit 15 ~ bit0

Reset: 00h

12.15. Signature Data Register

Address: 3C5H Index: 23-22 Access: RO

Bits 15:0 Signature data

12.16. Monitor Sense Register

Address: 3C5H Index: 25 Access: RO

Bits 7:6 Reserved

Bits 5:3 CRT2 DAC RGB monitor signal: [red, green, blue]

Bits 2:0 CRT1 DAC RGB monitor signal: [red, green, blue]

12.17. Video Key Mode

Address: 3C5H Index: 37 Access: Read/Write

Bit 7 Standard feature connector input mode clock polarity select:
0: normal
1: inverted

Bit 6 Signal output is sent:
0: before AFC processing;
1: after AFC processing

Bits 5:4 Feature connector input mode pixel clock timing tuning:
00: 0; 01: 4ns; 10: 8ns; 11: 12ns delay of pixel clock with respect to pixel data

Bits 3:0 Overlay key type:
0000: VGA port only
0001: Video key & Color key
0010: Color key & ~Video key
0011: Color key
0100: ~Color key & Video key
0101: Video key
0110: Color key XOR Video key
0111: Color key | Video key
1000: ~Color key & ~Video key
1001: Color key XNOR Video key
1010: ~Video key
1011: Color key | ~Video key
1100: ~Color key
1101: ~Color key | Video key
1110: ~Color key | ~Video key
1111: Video port only

Reset: 00h

12.18. Feature Connector Control Register

Address: 3C5H Index: 38 Access: Read/Write

Bits 7:4 X0X0: OLDDCLK0 = PCLK
 X0X1: OLDDCLK0 = PCLK, invert
 010X: OLDDCLK0 = 1/2PCLK
 011X: OLDDCLK0 = 1/2PCLK, invert
 11XX: OLDDCLK0 = 1/4PCLK, invert
 When 3D5.C1.bit3 = 0, DCLK0 = OLDDCLK0
 When 3D5.C1.bit3 = 1, DCLK0 = 1/2OLDDCLK0

Bits 3:0 Reserved

12.19. Playback Color Key Compare Data Register

Address: 3C5H Index: 52-50 Access: Read/Write

Bits 23:16 Playback color key for True Color mode

Bits 15:8 Playback color key for Hi-color mode

Bits 7:0 Playback color key for 256 color mode

12.20. Playback Color Key Mask Register

Address: 3C5H Index: 56-54 Access: Read/Write

Bits 23:16 Playback color key mask for True Color mode

Bits 15:8 Playback color key mask for Hi-color mode

Bits 7:0 Playback color key mask for 256 color mode

12.21. Playback Video Key Mode Function Select

Address: 3C5H Index: 57 Access: Read/Write

Bits 7:0 Overlay Key type, defining all 256 different types of mixing among VGA Color Key, playback window key, and Video Chroma Key. This code is very similar to ROP3 code.

Below are some most common combinations:

00: VGA port only
F0: Color key only
CC: Playback key only
AA: Chromakey only
88: Playback key & Chromakey
C0: Colorkey & Playback key
80: Colorkey & Playback key & Chromakey
FF: Video port only

Reset: 00h

12.22. 2nd Playback Color Key Compare Data

Address: 3C5H Index: 62-60 Access: Read/Write

Bits 23:16 Playback color key for True Color mode

Bits 15:8 Playback color key for Hi-color mode

Bits 7:0 Playback color key for 256 color mode

12.23. 2nd Playback Color Key Mask Register

Address: 3C5H Index: 66-64 Access: Read/Write

Bits 23:16 Playback color key mask for True Color mode

Bits 15:8 Playback color key mask for Hi-color mode

Bits 7:0 Playback color key mask for 256 color mode

13. Video Engine MMIO Registers (Base Addr. + 2400H)

13.1. Window1 starting address of Y frame buffer

Address: 24XXH Index: 03-00 Access: Read/Write

Bit 31 Window1 Starting address of Y frame buffer
0 = framebuffer mode
1 = framebufferless mode

Bits
30:25 Reserved

Bits 24:0 W1_ADDY<24:0>
Starting address of Y frame buffer for window1

13.2. Window1 starting address of U frame buffer

Address: 24XXH Index: 07-04 Access: Read/Write

Bits
31:25 Reserved

Bits 24:0 W1_ADDU<24:0>
Starting address of U frame buffer for window1

13.3. Window1 starting address of V frame buffer

Address: 24XXH Index: 0B-08 Access: Read/Write

Bits
31:25 Reserved

Bits 24:0 W1_ADDV<24:0>
Starting address of V frame buffer for window1

13.4. Window1 row byte of Y

Address: 24XXH Index: 0D-0C Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_RBOFFY<11:0>
Row byte of Y for window1 (128 bits alignment)

13.5. Window1 row byte of UV

Address: 24XXH Index: 0F-0E Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_RBOFFUV<11:0>
Row byte of UV for window1 (128 bits alignment)

13.6. Window1 Line Buffer Level

Address: 24XXH Index: 11-10 Access: Read/Write

Bits
15:10 Reserved

Bits 9:0 W1_LNBFLVL<9:0>
Window1 line buffer level

13.7. Window1 Line Buffer Threshold

Address: 24XXH Index: 12 Access: Read/Write

Bit 7 Reserved

Bits 6:0 W1_LNBFRQTH<6:0>
window1 line buffer request threshold

13.8. Window1 Horizontal Start

Address: 24XXH Index: 15-14 Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_HSTART<11:0>
window1 horizontal start

13.9. Window1 Horizontal End

Address: 24XXH Index: 17-16 Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_HEND<11:0>
window1 horizontal end

13.10. Window1 Vertical Start

Address: 24XXH Index: 19-18 Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_VSTART<11:0>
window1 vertical start

13.11. Window1 Vertical End

Address: 24XXH Index: 1B-1A Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W1_VEND<11:0>
window1 vertical end

13.12. Window1 Horizontal Scaling Factor

Address: 24XXH Index: 1D-1C Access: Read/Write

Bit 15 Reserved

Bits 14:0 W1_HZF<14:0>
window1 horizontal zoom factor

13.13. Window1 Vertical Scaling Factor

Address: 24XXH Index: 21-20 Access: Read/Write

Bit 15 Reserved

Bits 14:0 W1_VZF<14:0>
window1 vertical zoom factor

13.14. Window1 Misc. 1

Address: 24XXH Index: 28 Access: Read/Write

Bits 7:6 Reserved

Bit 5 W1_PMDX
Window1 horizontal Y/UV ratio
1: 4x (YUV411)
*0: 2x (YUV42x)

Bits 4:3 W1_PMDY<1:0>
Window1 vertical Y/UV ratio
*00: 2x (YUV420)
01: 4x (YUV410)
1x: 1x (YUV422)

Bits 2:0 W1_CMD<2:0>
Window1 data format
*000: YUV
010: RGB16
011: RGB15
100: RGB32 8-8-8-8
101: RGB32 CC mode
110: RGB32 AA mode
111: RGB32 2-10-10-10

13.15. Window1 Misc. 2

Address: 24XXH Index: 29 Access: Read/Write

Bits 7:5 Reserved

Bit 4 W1_CSCPASS
1: window1 RGB format
*0: window1 YUV format

Bit 3	W1_HSCBEN	1: Window1 HSCB enable *0: Window1 HSCB bypass
Bits 2:0	W1_MD<2:0>	Window1 window mode *000: YUV non-planar, LBUF mode 001: YUV planar but not NV12, LBUF mode 010: YUV non-planar or RGB, FIFO_mode 011: NV12, LBUF_mode 100: RGB LBUF mode

13.16. Window1 Misc. 3

Address: 24XXH Index: 2A Access: Read/Write

Bit 7	Reserved	
Bits 6:4	W1_HDEADJ<2:0>	Window1 HDE adjustment * The default value is 0H
Bit 3	W1_VMIRR	1: window1 vertical mirror enable 0: window1 vertical mirror disable
Bit 2	W1_HMIRR	1: window1 vertical mirror enable 0: window1 vertical mirror disable
Bit 1	W1_VINTEN	Window1 vertical interpolation disable 1: Disable *0: Enable
Bit 0	W1_HINTEN	Window1 horizontal interpolation disable 1: Disable *0: Enable

13.17. Window1 Sharp parameter

Address: 24XXH Index: 2B Access: Read/Write

Bits 7:0	W1_SHARP_PAR<7:0>	Window1 Sharp parameter
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13.18. Window1 Brightness Adjustment

Address: 24XXH Index: 2C Access: Read/Write

Bits 7:6	Reserved	
Bits 5:0	W1_BRIT<5:0>	Window1 Brightness Adjustment

13.19. Window1 Contrast Adjustment

Address: 24XXH Index: 2D Access: Read/Write

Bits 7:4 Reserved

Bits 3:0 W1_CONT<3:0>
window1 contrast adjustment

13.20. Window1 Hue and Saturation Adjustment

Address: 24XXH Index: 2E Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 W1_SHUS<4:0>
Window1 Hue * Sin(H) Adjustment

13.21. Window1 Hue and Saturation Adjustment

Address: 24XXH Index: 2F Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 W1_CHUS<4:0>
Window1 Hue * Cos(H) Adjustment

13.22. Window1 Misc. 4

Address: 24XXH Index: 30 Access: Read/Write

Bit 2 Reserved

Bits 1:0 FLICKEN1

13.23. Window1 Band/Pitch Control

Address: 24XXH Index: 33-32 Access: Read/Write

Bits W1_BANDM<1:0>
15:14 Surface1 Band Mode Control
11: Reserved
10: Surface1 Band 64x64
01: Surface1 Band 64x64 interleaved with Z
*00: Surface1 Linear Mode

Bits Reserved
13:10

Bits 9:0 W1_PITCH<9:0>
Window1 Band Mode Pitch (128 bit alignment, Total 10 bits)
* The default value is 00H

13.24. Window1 Panning X

Address: 24XXH Index: 35-34 Access: Read/Write

Bit 15	X_OFFSETEN	Window1 Panning X Offset active control 1: Active. *0: Inactive.
Bits 14:10	Reserved	
Bits 9:0	X_OFFSET<11:0>	Window1 Panning X Offset (128 bits alignment)

13.25. Window1 Panning Y

Address: 24XXH Index: 37-36 Access: Read/Write

Bit 15	Y_OFFSETEN	Window1 Panning Y Offset active control 1: Active. *0: Inactive.
Bits 14:10	Reserved	
Bits 9:0	Y_OFFSET<11:0>	Window1 Panning X Offset (128 bits alignment)

13.26. Window1 Color Key

Address: 24XXH Index: 3B-38 Access: Read/Write

Bits 31:30	Reserved	
Bits 29:0	W1_KEYCOLOR<29:0>	Widow1 Color Key RGB 10-10-10 Value

13.27. Window1 Color Key Mask

Address: 24XXH Index: 3F-3C Access: Read/Write

Bits 31:30	Reserved	
Bits 29:0	W1_KEYMASK<29:0>	Widow1 Color Key Mask

13.28. Window1 Playback Key Mode Function Select

Address: 24XXH Index: 40 Access: Read/Write

Bits 7:0 W1_PBKEYSEL<7:0>

Play back key mode function select control for window1

*00: VGA only

FF: Video port only

F0: Color key only

CC: Window (playback) key only

AA: Chroma key only

88: Window key & Chroma key

C0: Color key & Window key

80: Color key & Window key & Chroma key

* The default value is 00H

13.29. Window1 Constant Alpha

Address: 24XXH Index: 41 Access: Read/Write

Bits 9:0 W1_CALPHA<7:0>

* The default value is 00H

13.30. Window1 Overlay/Blending Control

Address: 24XXH Index: 42 Access: Read/Write

Bits 7:6 Reserved

Bit 5 MC4

Window1 CRTC Selection

1: 2nd CRTC

*0: 1st CRTC

Bit 4 W1_ENCOLORKEY

Enable Window1 Color Key

1: Enable

*0: Disable

Bit 3 W1_PREMUTI

Enable Window1 Alpha Pre-Multiplied

1: Enable

*0: Disable

Bit 2 W1_SKEYPOL

Window1 Source Key Polarity

1: Keep while Surface 1 Source color inside range

*0: Kill while Surface 1 Source color inside range

Bit 1 W1_CALPHAEN

Enable Window 1 Constant Alpha Blending

1: Enable

*0: Disable

Bit 0	W1_ALPHAEN	Enable Window1 <u>pixel by pixel</u> Alpha Blending
		1: Enable
		*0: Disable

13.31. Window1 Source Key Lower Bound

Address: 24XXH Index: 46-44 Access: Read/Write

Bits 23:0	W1_KEYDATA<23:0>
	Window1 Source Key Lower Bound

13.32. Window1 Source Key Upper Bound

Address: 24XXH Index: 4A-48 Access: Read/Write

Bits 23:0	W1_KEYDATAH<23:0>
	Window1 Source Key Upper Bound

13.33. Window1 Overlay/Blending Control

Address: 24XXH Index: 50 Access: Read/Write

Bit 7	EDGEEN	Window1 Edge recovery algorithm control
		1: Enable
		*0: Disable
Bits 6:3	Reserved	
Bit 2	SYNCSEL	
Bit 1	LNBFTOG	Line toggle for line buffer
		1: Toggle(Reversed)
		*0: Normal
Bit 0	CIRDTV	CCIR-DTV input video data format control
		1: DTV Format
		*0: CCIR Format

13.34. Window1 Edge Threshold

Address: 24XXH Index: 51 Access: Read/Write

Bits 7:5	Text threshold
Bit 4	Text procedure enable
	1: Enable 0: Disable
Bit 3	1: 5 median 0: 3 median filter
Bits 2:1	Direction select
	00:3 01:5 1x:7 directions
Bit 0	EDGE judgment control

13.35. New MD Cont

Address: 24XXH Index: 53-52 Access: Read/Write

Bits 15:0 NEW_MD_CONT<15:0>
EDGE judgment threshold

13.36. MOT_THRES

Address: 24XXH Index: 57-54 Access: Read/Write

Bits MOT_THRES<2:0>
31:29 Motion Threshold
010 : 2
011 : 4
100 : 8
101 : 16
110 : 32

Bits Reserved
28:25

Bits 4:0 DISADDPY1<24:0>
Starting address of previous frame

13.37. Window1 Misc. 5

Address: 24XXH Index: 58 Access: Read/Write

Bit 7 BOTTOM_SEL
*0: internal starting address switch between original setting and
shift one row byte every field
1: internal starting address switch depends on TOPFIRST
setting

Bits 6 TOPFIRST
*0: bottom field first
1: top field first

Bits 5:4 DISP_MODE
*00: internal starting address is same as register setting
01: internal starting address shift one row byte for interleaved
odd field data
1x: enable internal starting address switch

Bit 3 BOBWEAVE_DBF
0 : double buffer(BOB or DEINT) 1 : Weave

Bit 2 BOBWEAVE

Bit 1 ENYBLINE
When DEINT and 3:2 enabled

Bit 0 DEINTEN
1: de-interlace enable
0: de-interlace disable

13.38. Window1 line buffer level

Address: 24XXH Index: 59 Access: Read/Write

Bit 7	PANORAMAEN Enable Window 1 Panorama 1: Enable *0: Disable
Bits 6:2	Reserved
Bits 1:0	MOTION_FACTOR<1:0> The final output is from TEXT procedure or median filter or both 00 TEXT proc 01 Median filter 1x (TEXT_PROC + Median) / 2

13.39. Panorama Horizontal Scaling Factor1

Address: 24XXH Index: 5B-5A Access: Read/Write

Bits 15:14	Reserved
Bits 13:0	PANA_HZF1

13.40. Panorama Horizontal Scaling Factor2

Address: 24XXH Index: 5D-5C Access: Read/Write

Bits 15:14	Reserved
Bits 13:0	PANA_HZF2

13.41. Panorama Horizontal Scaling Factor3

Address: 24XXH Index: 5F-5E Access: Read/Write

Bits 15:14	Reserved
Bits 13:0	PANA_HZF3

13.42. Panorama HCNT1

Address: 24XXH Index: 61-60 Access: Read/Write

Bits 15:14	Reserved
Bits 13:0	PANA_HCNT1

13.43. Panorama HCNT2

Address: 24XXH Index: 63-62 Access: Read/Write

Bits Reserved
15:14

Bits 13:0 PANA_HCNT2

13.44. Panorama HCNT3

Address: 24XXH Index: 65-64 Access: Read/Write

Bits Reserved
15:14

Bits 13:0 PANA_HCNT3

13.45. Panorama HCNT4

Address: 24XXH Index: 67-66 Access: Read/Write

Bits Reserved
15:14

Bits 13:0 PANA_HCNT4

13.46. Panorama HCNT5

Address: 24XXH Index: 69-68 Access: Read/Write

Bits Reserved
15:14

Bits 13:0 PANA_HCNT5

13.47. Panorama HCNT6

Address: 24XXH Index: 6B-6A Access: Read/Write

Bits Reserved
15:14

Bits 13:0 PANA_HCNT6

13.48. Window1 Misc. 6

Address: 24XXH Index: 6F-6C Access: Read/Write

Bit 31 W1_ENDDBA

Bit 30 SOFTOE

Bits Reserved
29:25

Bits 24:0 W1_ADDY2

13.49. Window1 Misc. 7

Address: 24XXH Index: 70 Access: Read/Write

Bits 7:4	Reserved
Bit 3	MCINTODD_POL
Bit 2	SPFORMAT sub-picture format 1: DATAB2<7:4> for sub-picture index DATAB2<3:0> for sub-picture blending factor 0: DATAB2<7:4> for sub-picture blending factor DATAB2<3:0> for sub-picture index
Bit 1	SUBPICEN 1: sub-picture enable 0: sub-picture disable
Bit 0	ENMC 1: Motion Compensation Enable. *0: Motion Compensation disable.

13.50. Window1 LCD Overdrive Write Back Frame Buffer Start Address

Address: 24XXH Index: 77-74 Access: Read/Write

Bits 31:25	Window 1 LCD Overdrive Write Back Frame Buffer Start Address <i>Reserved</i>
Bits 24:0	LOD_STADD<24:0> (128 bits alignment)

13.51. Window1 LOD_LUT_DIN

Address: 24XXH Index: 7A-78 Access: Read/Write

Bits 23:0 Overdrive LUT Data Write Bus, each time fill in 4 cells

13.52. Window1 LCD Overdrive

Address: 24XXH Index: 7C-7B Access: Read/Write

Bit 15	LODEN Enable Window1 LCD Overdrive function 1: Enable *0: Disable
Bits 14:12	Reserved
Bit 11	LOD_DIV2 Overdrive LUT content value divided by 2. i.e. {Content, 2'b0} => {1'b0, Content, 1'b0}

Bit 10	LOD_LUT_WEB Overdrive LUT Write Enable 1: Read Only *0: Write only
Bits 9:0	LOD_LUT_AIN<9:0> Overdrive LUT Address Write Bus. Higher two bits are used to select one of four 32x32 LUT.

13.53. Write/Read Buffer Watermark

Address: 24XXH Index: 7D Access: Read/Write

Bits 7:4	WBUF_WATERMARK<3:0> Overdrive Write Buffer Water Mark
Bits 3:0	RBUF_WATERMARK<3:0> Overdrive Read Buffer Water Mark

13.54. Window1 Vertical Scan Line Number

Address: 24XXH Index: 7F-7E Access: Read Only

Bits 15:12	Reserved
Bits 11:0	VCOUNT1<11:0> Window 1 Vertical Scan Line Number

13.55. Window2 starting address of Y frame buffer

Address: 24XXH Index: 83-80 Access: Read/Write

Bit 31	Window2 Starting address of Y frame buffer 0 = framebuffer mode 1 = framebufferless mode
Bits 30:25	Reserved
Bits 24:0	W2_ADDY<24:0> Starting address of Y frame buffer for window2

13.56. Window2 starting address of U frame buffer

Address: 24XXH Index: 87-84 Access: Read/Write

Bits 31:25	Reserved
Bits 24:0	W2_ADDU<24:0> Starting address of U frame buffer for window2

13.57. Window2 starting address of V frame buffer

Address: 24XXH Index: 8B-88 Access: Read/Write

Bits
31:25 Reserved

Bits 24:0 W2_ADDV<24:0>
Starting address of V frame buffer for window2

13.58. Window2 row byte of Y

Address: 24XXH Index: 8D-8C Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W2_RBOFFY<11:0>
Row byte of Y for window2 (128 bits alignment)

13.59. Window2 row byte of UV

Address: 24XXH Index: 8F-8E Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W2_RBOFFUV<11:0>
Row byte of UV for window2 (128 bits alignment)

13.60. Window2 Line Buffer Level

Address: 24XXH Index: 91-90 Access: Read/Write

Bits
15:10 Reserved

Bits 9:0 W2_LNBFLVL<9:0>
Window2 line buffer level

13.61. Window2 Line Buffer Threshold

Address: 24XXH Index: 92 Access: Read/Write

Bit 7 Reserved

Bits 6:0 W2_LNBFRQTH<6:0>
window2 line buffer request threshold

13.62. Window2 Horizontal Start

Address: 24XXH Index: 95-94 Access: Read/Write

Bits
15:12 Reserved

Bits 11:0 W2_HSTART<11:0>
window2 horizontal start

13.63. Window2 Horizontal End

Address: 24XXH Index: 97-96 Access: Read/Write

Bits 15:12	Reserved
Bits 11:0	W2_HEND<11:0> window2 horizontal end

13.64. Window2 Vertical Start

Address: 24XXH Index: 99-98 Access: Read/Write

Bits 15:12	Reserved
Bits 11:0	W2_VSTART<11:0> window2 vertical start

13.65. Window2 Vertical End

Address: 24XXH Index: 9B-9A Access: Read/Write

Bits 15:12	Reserved
Bits 11:0	W2_VEND<11:0> window2 vertical end

13.66. Window2 Horizontal Scaling Factor

Address: 24XXH Index: 9D-9C Access: Read/Write

Bit 15	Reserved
Bits 14:0	W2_HZF<14:0> window2 horizontal zoom factor

13.67. Window2 Vertical Scaling Factor

Address: 24XXH Index: A1-A0 Access: Read/Write

Bit 15	Reserved
Bits 14:0	W2_VZF<14:0> window2 vertical zoom factor

13.68. Window2 Misc. 1

Address: 24XXH Index: A8 Access: Read/Write

Bits 7:6	Reserved
Bit 5	W2_PMDX Window2 horizontal Y/UV ratio 1: 4x (YUV411) *0: 2x (YUV42x)

Bits 4:3	W2_PMDY<1:0> Window2 vertical Y/UV ratio *00: 2x (YUV420) 01: 4x (YUV410) 1x: 1x (YUV422)
Bits 2:0	W2_CMD<2:0> Window2 data format *000: YUV 010: RGB16 011: RGB15 100: RGB32 8-8-8-8 101: RGB32 CC mode 110: RGB32 AA mode 111: RGB32 2-10-10-10

13.69. Window2 Misc. 2

Address: 24XXH Index: A9 Access: Read/Write

Bits 7:5	Reserved
Bit 4	W2_CSCPASS 1: window2 RGB format *0: window2 YUV format
Bit 3	W2_HSCBEN 1: Window2 HSCB enable *0: Window2 HSCB bypass
Bits 2:0	W2_MD<2:0> Window2 window mode *000: YUV non-planar, LBUF mode 001: YUV planar but not NV12, LBUF mode 010: YUV non-planar or RGB, FIFO_mode 011: NV12, LBUF_mode 100: RGB LBUF mode

13.70. Window2 Misc. 3

Address: 24XXH Index: AA Access: Read/Write

Bit 7	Reserved
Bits 6:4	W2_HDEADJ<2:0> Window2 HDE adjustment * The default value is 0H
Bit 3	W2_VMIRR 1: window2 vertical mirror enable 0: window2 vertical mirror disable
Bit 2	W2_HMIRR 1: window2 vertical mirror enable 0: window2 vertical mirror disable

Bit 1	W2_VINTEN	Window2 vertical interpolation disable 1: Disable *0: Enable
Bit 0	W2_HINTEN	Window2 horizontal interpolation disable 1: Disable *0: Enable

13.71. Window2 Sharp parameter

Address: 24XXH Index: AB Access: Read/Write

Bits 7:0	W2_SHARP_PAR<7:0>	Window2 Sharp parameter
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13.72. Window2 Brightness Adjustment

Address: 24XXH Index: AC Access: Read/Write

Bits 7:6	Reserved	
Bits 5:0	W2_BRIT<5:0>	Window2 Brightness Adjustment

13.73. Window2 Contrast Adjustment

Address: 24XXH Index: AD Access: Read/Write

Bits 7:4	Reserved	
Bits 3:0	W2_CONT<3:0>	window2 contrast adjustment

13.74. Window2 Hue and Saturation Adjustment

Address: 24XXH Index: AE Access: Read/Write

Bits 7:5	Reserved	
Bits 4:0	W2_SHUS<4:0>	Window2 Hue * Sin(H) Adjustment

13.75. Window2 Hue and Saturation Adjustment

Address: 24XXH Index: AF Access: Read/Write

Bits 7:5	Reserved	
Bits 4:0	W2_CHUS<4:0>	Window2 Hue * Cos(H) Adjustment

13.76. Window2 Misc. 4

Address: 24XXH Index: B0 Access: Read/Write

Bit 2	Reserved	
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Bits 1:0 FLICKEN1

13.77. Window2 Band/Pitch Control

Address: 24XXH Index: B3-B2 Access: Read/Write

Bits W2_BANDM<1:0>
15:14 Surface1 Band Mode Control
 11: Reserved
 10: Surface1 Band 64x64
 01: Surface1 Band 64x64 interleaved with Z
 *00: Surface1 Linear Mode

Bits Reserved
13:10

Bits 9:0 W2_PITCH<9:0>
 Window2 Band Mode Pitch (128 bit alignment, Total 10 bits)
 * The default value is 00H

13.78. Window2 Panning X

Address: 24XXH Index: B5-B4 Access: Read/Write

Bit 15 X_OFFSETEN
 Window2 Panning X Offset active control
 1: Active.
 *0: Inactive.

Bits Reserved
14:10

Bits 9:0 X_OFFSET<11:0>
 Window2 Panning X Offset (128 bits alignment)

13.79. Window2 Panning Y

Address: 24XXH Index: B7-B6 Access: Read/Write

Bit 15 Y_OFFSETEN
 Window2 Panning Y Offset active control
 1: Active.
 *0: Inactive.

Bits Reserved
14:10

Bits 9:0 Y_OFFSET<11:0>
 Window2 Panning X Offset (128 bits alignment)

13.80. Window2 Color Key

Address: 24XXH Index: BB-B8 Access: Read/Write

Bits Reserved
31:30

Bits 29:0 W2_KEYCOLOR<29:0>
Widow2 Color Key RGB 10-10-10 Value

13.81. Window2 Color Key Mask

Address: 24XXH Index: BF-BC Access: Read/Write

Bits
31:30 Reserved

Bits 29:0 W2_KEYMASK<29:0>
Widow2 Color Key Mask

13.82. Window2 Playback Key Mode Function Select

Address: 24XXH Index: C0 Access: Read/Write

Bits 7:0 W2_PBKEYSEL<7:0>
Play back key mode function select control for window2
*00: VGA only
FF: Video port only
F0: Color key only
CC: Window (playback) key only
AA: Chroma key only
88: Window key & Chroma key
C0: Color key & Window key
80: Color key & Window key & Chroma key
* The default value is 00H

13.83. Window2 Constant Alpha

Address: 24XXH Index: C1 Access: Read/Write

Bits 9:0 W2_CALPHA<7:0>
* The default value is 00H

13.84. Window2 Overlay/Blending Control

Address: 24XXH Index: C2 Access: Read/Write

Bits 7:6 Reserved

Bit 5 MC5
Window2 CRTC Selection
1: 2nd CRTC
*0: 1st CRTC

Bit 4 W2_ENCOLORKEY
Enable Window2 Color Key
1: Enable
*0: Disable

Bit 3 W2_PREMUTI
Enable Window2 Alpha Pre-Multiplied
1: Enable
*0: Disable

Bit 2	W2_SKEYPOL	Window2 Source Key Polarity 1: Keep while Surface 1 Source color inside range *0: Kill while Surface 1 Source color inside range
Bit 1	W2_CALPHAEN	Enable Window 1 <u>Constant</u> Alpha Blending 1: Enable *0: Disable
Bit 0	W2_ALPHAEN	Enable Window2 <u>pixel by pixel</u> Alpha Blending 1: Enable *0: Disable

13.85. Window2 Source Key Lower Bound

Address: 24XXH Index: C6-C4 Access: Read/Write

Bits 23:0 W2_KEYDATA<23:0>
Window2 Source Key Lower Bound

13.86. Window2 Source Key Upper Bound

Address: 24XXH Index: CA-C8 Access: Read/Write

Bits 23:0 W2_KEYDATAH<23:0>
Window2 Source Key Upper Bound

13.87. Window2 Misc. 4

Address: 24XXH Index: D0 Access: Read/Write

Bits 7:2	Reserved
Bit 1	ENBORDER Enable Window2 Scaling Border Garbage Fix 1: Enable *0: Disable
Bit 0	UV_UPSAMPLEEN 1: UV sample enable 0: UV sample disable

13.88. Window2 Misc. 5

Address: 24XXH Index: D1 Access: Read/Write

Bits 7:3	Reserved
Bit 2	VAHC_TRIPLE10 Enable Video Alpha Cursor 2-10-10-10 Mode 1: Enable *0: Disable

Bit 1	VAHC_TRCOLOR	Enable Video Alpha Cursor 8-8-8 Mode 1: Enable *0: Disable
Bit 0	VAHCEN	Enable Video Alpha Cursor 1: Enable *0: Disable

13.89. Video Alpha Cursor Pitch

Address: 24XXH Index: D3-D2 Access: Read/Write

Bits 15:10	Reserved
Bits 9:0	VHCPITCH<9:0> Video Alpha Cursor Pitch (128 bits alignment)

13.90. Video Alpha Cursor Start Address

Address: 24XXH Index: D7-D4 Access: Read/Write

Bits 31:25	Reserved
Bits 24:0	VHCPITCH<9:0> Video Alpha Cursor Pitch (128 bits alignment)

13.91. Window1 ENDBA

Address: 24XXH Index: EF Access: Read/Write

Bit 7	W1_ENDBA
Bits 6:0	Reserved

14. Video Capture & 3-to-2 Detection MMIO Registers (Base Addr. + 25XX)

14.1. Video Window Horizontal Start

Address: 25XXH Index: 01-00 Access: Read/Write

Bits 15:13 Reserved

Bits 12:0 CHSTART<12:0>

14.2. Video Window Horizontal End

Address: 25XXH Index: 03-02 Access: Read/Write

Bits 15:13 Reserved

Bits 12:0 CHEND<12:0>

14.1. Video Window Vertical Start

Address: 25XXH Index: 05-04 Access: Read/Write

Bits 15:13 Reserved

Bits 12:0 CVSTART<12:0>

14.2. Video Window Vertical End

Address: 25XXH Index: 07-06 Access: Read/Write

Bits 15:13 Reserved

Bits 12:0 CVEND<12:0>

14.3. Horizontal Sync Width

Address: 25XXH Index: 08 Access: Read/Write

Bits 7:0 CHSWIDTH<7:0>

14.4. Vertical Sync Width

Address: 25XXH Index: 09 Access: Read/Write

Bits 7:0 CVSWIDTH<7:0>

14.5. Misc. Control 0

Address: 25XXH Index: 0A Access: Read/Write

Bit 7	CVDESEL	
		1: VDE from external
		*0: VDE generated by internal CRTC
Bit 6	CHDESEL	
		HDE select
		1: HDE from external port
		*0: HDE generated by internal CRTC
Bit 5	CAPSWAPEN	
		Capture address swap enable
Bit 4	CAPSWAP	
		Capture address swap
Bit 3	CAPEOSEL	
		Field EVEN/ODD generator select
Bit 2	CAPEOINV	
		Field Even/Odd Invert
Bit 1	CVSP	
		Vertical Sync Pulse Polarity
Bit 0	CHSP	
		Horizontal Sync Pulse Polarity

14.6. Misc. Control 1

Address: 25XXH Index: 0B Access: Read/Write

Bits 7:6	Reserved	
Bit 5	ENCINT	
		Enable Capture Interrupt
Bits 4:3	CINTSRC	
		*00: CAP_VSYNC; 01: VDE; 1x: Field
Bit 3	CLRCINT	
		Clear interrupt signal
		1: clear the interrupt signal
		*0: keep the signal
Bit 2	CAPEOINV	
		Field Even/Odd Invert

Bit 1 CEXTSYNCEN
 1: 656 Video HS, VS come from external port
 *0: 656 video HS, VS decoded from video data

Bit 0 CFLICKEN
 Set to “1” for flicker-free function when input is in the
 interlaced mode

14.7. Misc. Control 2

Address: 25XXH Index: 0D-0C Access: Read/Write

Bits 15:9 Reserved

Bits 8:0 FRONTPORCH656<8:0>
 The front porch for 656 format video data.
 **The default value is 000h, Need SW set 9d'208 as default.*

14.8. Misc. Control 3

Address: 25XXH Index: 11-10 Access: Read/Write

Bits 15:14 Reserved

Bits 13:0 CROWBYTE<13:0>
 Capture Row byte

14.9. Misc. Control 4

Address: 25XXH Index: 12 Access: Read/Write

Bit 7 AUDIOEN
 Audio data capture enable

Bit 6 EN656
 656 format data input enable
 1: Enable
 *0: Disable

Bit 5 SINGLE_EDGE
 Latch the external video data in single edge

Bit 3 TV8BIT
 Support low 8 bit data input

Bit 2 ADDREG
 1: address generate in new way
 *0: address generate in old way

Bit 1	WEAVE	1: Weave mode *0: Bob mode
Bit 0	ANTITEAR	Enable Anti-tearing function 1: anti-tearing enable *0: anti-tearing disable

14.10. Misc. Control 5

Address: 25XXH Index: 13 Access: Read/Write

Bits 7:6	CAPMODE<1:0>	Frame Capture control *00: Interlace capture 01: Even/Odd 60fs capture 10: Even field 30fs capture 11: ODD field 30fs capture
Bits 5:4	COLORMD<1:0>	Capture input data mode: *00: YUV 422 01: YUV 411 10: RGB656 11: Reserved
Bit 3	CAPCIRDTV	Capture DTV/CCIR format select: 1: DTV *0: CCIR
Bit 2	UV9051	Philips UV9051 format select 1: UV9051 format *0: normal
Bit 1	UVIV	U,V Swap 1: swap *0: normal

Bit 0 YUVIV
 Y,UV swap
 1: swap
 *0: normal

14.11. Misc. Control 6

Address: 25XXH Index: 14 Access: Read/Write

Bit 7 DBLINE
 At interlace mode:
 1: one line drop
 *0: double line drop

Bits 6:4 CDITHMD<2:0>
 Dithering mode
 * 000: bypass dithering
 001: 24 chop to 16 bpp
 010: 24 bpp to 16 bpp

Bit 3 CAPCSCEN
 Color space convert enable
 1: Enable
 *0: Disable

Bits 2:0 FILTMD<2:0>
 Horizontal Filter TAP:
 *0XX: Bypass
 100: 2 TAP
 101: 3 TAP
 110: 5 TAP
 111: 9 TAP

14.12. Misc. Control 7

Address: 25XXH Index: 15 Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 CRQTH1<4:0>
 Capture FIFO request threshold control

14.13. Misc. Control 8

Address: 25XXH Index: 16 Access: Read/Write

Bits 7:6 CPBK1<1:0>
Capture FIFO page break
*00: 8 level
01: 16 level
1X: 32 level

Bits 5:0 CLVL1<5:0>
Capture FIFO level control

14.14. Capture MPEG Mode Control

Address: 25XXH Index: 17 Access: Read/Write

Bits 7:3 Reserved

Bit 2 ENMEG

Bits 1:0 MPEG_INTMODE

14.15. Misc. Control 9

Address: 25XXH Index: 19-18 Access: Read/Write

Bits 15:10 Reserved

Bits 9:0 CVMF<9:0>
Vertical Minify Factor
*The default value is 000h, Need SW set 3FFh as default

14.16. Misc. Control 10

Address: 25XXH Index: 1B-1A Access: Read/Write

Bits 15:10 Reserved

Bits 9:0 CHMF<9:0>
Horizontal Minify Factor
*The default value is 000h, Need SW set 3FFh as default

14.17. Misc. Control 11

Address: 25XXH Index: 1F-1C Access: Read/Write

Bits 31:25 Reserved

Bits 24:0 AUDIO_STADD<24:0>
Audio data memory start address

14.18. Misc. Control 12

Address: 25XXH Index: 20 Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 CRQTH2<4:0>
Audio Data Capture FIFO request threshold control

14.19. Misc. Control 13

Address: 25XXH Index: 21 Access: Read/Write

Bits 7:6 CPBK2<1:0>
Audio Capture FIFO page break
*00: 8 level
01: 16 level
1X: 32 level

Bits 5:0 CLVL2<5:0>
Audio capture FIFO level control

14.20. Misc. Control 14

Address: 25XXH Index: 22 Access: Read/Write

Bits 7:2 Reserved
Bit 1 CLRACNT
AFORMAT
Bit 0

14.21. Misc. Control 15

Address: 25XXH Index: 43-40 Access: Read/Write

Reserved
Bits 31:26
Bits 25:0 MVDETCURR
3:2 Detection Current Address<QW address>

14.22. Misc. Control 16

Address: 25XXH Index: 47-44 Access: Read/Write

Reserved
Bits 31:26
Bits 25:0 MVDETPRD
3:2 Detection Previous Field Address<QW address>

14.23. Misc. Control 17

Address: 25XXH Index: 4B-48 Access: Read/Write

Reserved
Bits 31:26
Bits 25:0 MVDETPFR
3:2 Detection Previous Frame Address<QW address>

14.24. Misc. Control 18

Address: 25XXH Index: 4F-4C Access: Read/Write

Bits 31:26 Reserved

Bits 25:0 MVDETPFR

3:2 Detection Previous Frame Address<QW address>

14.25. Misc. Control 19

Address: 25XXH Index: 53-50 Access: Read/Write

Bit 31 SW Reset

Bits 30:28 DUMMY[2:0]

Bit 27 Current FB #. =0 FB1, =1 FB2

Bit 26 3:2 detection enable

Bits 25:24 LPF TAP #

Bit 23 Bypass LPF. = 1 bypass

Bits 22:16 Picture width. (Frame Width /16)

Bits 15:7 Picture High. (Frame High / 4)

Bits 6:4 DVD FB #. =0: 1st FB, ..., =7: 8th FB

Bit 3 =1: Field Picture<YUV 420→422>

Bit 2 =1: Frame output<YUV420→YUV422>

Bit 1 =1: current field = top field

Bit 0 =1 Enable YUV420→YUV422

14.26. Misc. Control 20

Address: 25XXH Index: 57-54 Access: Read/Write

Bits 31:30 Frame_Weighted_Average_Number[1:0]

Bits 29:24 Frame_Motion_Thres[5:0]

Bits 23:12 MV_HEND[11:0]

Bits 11:0 MV_HSTART[11:0]

14.27. Misc. Control 21

Address: 25XXH Index: 5B-58 Access: Read/Write

Bits 31:30 Field_Weighted_Average_Number[1:0]

Bits 29:24 Field_Motion_Thres[5:0]

Bits 23:12 MV_VEND[11:0]
Bits 11:0 MV_VSTART[11:0]

14.28. Misc. Control 22

Address: 25XXH Index: 5B-58 Access: Read/Write

Bits 31:30 Field_Weighted_Average_Number[1:0]
Bits 29:24 Field_Motion_Thres[5:0]
Bits 23:12 MV_VEND[11:0]
Bits 11:0 MV_VSTART[11:0]

14.29. Misc. Control 23

Address: 25XXH Index: 5F-5C Access: Read/Write

Bits 31:29 Field_Adap_Thres_Factor[2:0]
Bits 28:26 Frame_Adap_Thres_Factor[2:0]
Bits 25:16 Minimum_Frame_Thres[9:0]
Bits 15:0 Maximum_Frame_Thres[15:0]

14.30. Misc. Control 24

Address: 25XXH Index: 63-60 Access: Read/Write

Bits 31:30 Cap_Timing_Invert[1:0]
Bits 29:28 Segment[1:0]
Bits 27:18 Minimum_Field_Thres[9:0]
Bits 17:0 Content_Change_Thres[17:0]

14.31. Misc. Control 25

Address: 25XXH Index: 67-64 Access: Read/Write

Bit 31 Bottom_First_Display
Bit 30 Field_Motion_0_Tighter
Bit 29 Frame_Motion_0_Tighter
Bit 28 Display_Quit_Enable
Bit 27 Field_Quit_Enable
Bit 26 Frame_Quit_Enable
Bit 25 Field_enter_Enable
Bit 24 Frame_Enter_Enable

Bits 23:22	Field_Quit_Ratio[1:0]
Bits 21:20	Field_Movie_Number[1:0]
Bits 19:18	Frame_Movie_Number[1:0]
Bits 17:0	Minimum_Scene_Change_Frame_Motion[17:0]

15. PCIE/Generic MMIO Registers (Base Addr. + 23XX)

15.1. Generic Channel Starting Address (System Memory)

Address: 000H Index: 43-40 Access: Read/Write

Bits 31:12	Starting address, 4KB aligned
Bit 9	Complete status
Bit 8	Enable generic channel
Bit 7	Data direction. =1: System memory to FB. =0: FB to system memory
Bit 6	Enable generic channel address protection.
Bit 5	Enable DVD channel address protection.
Bit 4	Local generic channel maximum read length control enable.
Bits 3:0	Read length. (2QW). driver need to make sure not to exceed the maximum read length allowed by PCIE.

15.2. Generic Channel Starting Address (Frame Buffer)

Address: 000H Index: 47-44 Access: Read/Write

Bits 31:25	Reserved
Bits 24:0	Starting address, 128-bit address.

15.3. X/Y Width/Height

Address: 000H Index: 4B-48 Access: Read/Write

Bits 31:16	Number of 128-bit data in X-direction need to be transferred.
Bits 15:0	Number of 128-bit data in Y-direction need to be transferred.

15.4. PCIE Pitch

Address: 000H Index: 4F-4C Access: Read/Write

Bits 31:18	Reserved
Bits 17:0	System side number of 128-bit in X-direction

15.5. Misc. Internal Register

Address: 000H Index: 5F-58 Access: Read/Write

Bit 31	DVD reset status, read only
Bit 30	Generic channel reset status, read only

Bit 29	GE reset status, read only
Bit 28	CPURD reset status, read only
Bit 27	DVD reset
Bit 26	Generic channel reset
Bit 25	GE channel reset
Bits 24:0	Reserved

16. PCIE Configuration Registers (000~167H)

16.1. Vendor and Device ID

Address: 000H Index: 03-00 Access: Read

Bits 31:16	Device ID
Bits 15:0	Vendor ID

16.2. Commnad and Status Register

Address: 004H Index: 03-00 Access: Read/Write

Bit 31	Detected Parity Error(RW1C) 0: Not detected, 1: Detected, set whenever the device receives a Poisoned TLP.
Bit 30	Signaled System Error (RW1C) 0: Not detected 1: Detected, set when the device sends an ERR_FATAL or ERR_NONFATAL msg.
Bit 29	Received Master Abort (RW1C) 0: normal 1: receive a Completion with Unsupported Request Cpl Status.
Bit 28	Received Target Abort (RW1C) 0: normal 1: receive a Completion with Completer Abort Cpl. Status
Bit 27	Signaled target abort (RW1C) 0: normal 1: completes a Request using Completer Abort Cpl. status
Bits 26:25	DEVSEL* timing (RO) Hardwired to 0
Bit 24	Master Data Parity Error (RW1C) 0: Not detected 1: Detected, set when the device receives a Cpl. marked poisoned and the Parity Error Enable bit is set.
Bit 23	Fast back-to-back capable (RO) 0: Hardwire to
Bit 22	Reserved
Bit 21	66 MHz capable (RO) 0: Hardwire to 0

Bit 20	Capabilities List (RO) 1: implements a list of capabilities (must set to 1)
Bit 19	Interrupt Status (RO) 0: No INTx interrupt Message is pending 1: An INTx interrupt Message is pending
Bits 18:11	Reserved
Bit 10	Interrupt Disable (RW) 0: Enable 1: Disable
Bit 9	Fast back-to-back enable (RO) 0: Hardwire to 0
Bit 8	SERR Enable (RW) 0: Disable 1: Enable (reporting of Non-fatal and Fatal errors detected by the device to the RC)
Bit 7	IDSEL Stepping00-03Wait Cycle Control (RO) 0: Hardwire to 0
Bit 6	Parity Error Enable (RW) 0: Disable 1: Enable
Bit 5	VGA Palette Snoop (RO) 0: Hardwire to 0
Bit 4	Memory write and invalidate enable (RO) 0: Hardwire to 0
Bit 3	Special cycles (RO) 0: Hardwire to 0
Bit 2	Bus Master (RW) 0: Device is not a bus master 1: Device is a bus master, which is able to issue Mem or IO Requests.
Bit 1	Memory Space (RW) 0: Disable 1: Enable the device to process Mem Requests
Bit 0	I/O Space 1: Enable *0: Disable

16.3. Revision ID and Class Code Register

Address: 008H Index: 03:00 Access: Read

Bits 31:8	Class Code (= 030000h)
Bits 7:0	Revision ID (= 00h) (The revision ID is depend on the chip version)

16.4. Cache Line and BIST Register

Address: 00CH Index: 03-00 Access: Read/Write

Bit 31	BIST capable (RO) 0: not capable 1: capable (hardwired to 1)
Bit 30	Start BIST 0: BIST stop/ BIST completed (Hardwire to 0) 1: invoke BIST (for internal test only)
Bits 29:28	Reserved
Bits 27:24	Completion Code 0000: BIST test passed (Hardwire to 0000) others: test failure code (for internal test only)
Bit 23	Multi-function device Hardwire to 0
Bits 22:16	Reserved
Bits 15:8	Hardwire to 0
Bits 7:0	Cache Line Size (RW)

16.5. Memory Base Address Register

Address: 010H Index: 03-00 Access: Read/Write

Bits 31:28	Memory Base address[31:28] 32-bit memory base register for 256MB linear frame buffer
Bit 27	128M Memory Base address
Bits 26:4	Memory Base address[26:4] (RO) 0: default value
Bit 3	Prefetchable (RO) 1: enable (default)
Bits 2:1	Addressing type (RO) 00: 32-bit address space (default)
Bit 0	Memory space indicator (RO)

0:

16.6. MMIO Base Address Register

Address: 014H Index: 03:00 Access: Read/Write

Bits 31:18	MMIO Base address[31:18] 32-bit memory base register for 128KB frame buffer
Bits 17:4	MMIO Base address[176:4] (RO) 0: default value
Bit 3	Prefetchable (RO) 1: enable (default)
Bits 2:1	Addressing type (RO) 00: 32-bit address space (default)
Bit 0	Memory space indicator (RO) 0: memory space (default)

16.7. Relocate IO Base Address Register

Address: 018H Index: 03:00 Access: Read/Write

Bits 31:7	Subsystem ID
Bits 6:1	Subsystem Vendor ID
Bit 0	Memory space indicator (RO)

16.8. Subsystem Vendor and ID Register

Address: 02CH Index: 03:00 Access: Read/Write

Bits 31:16	Subsystem ID
Bits 15:0	Vendor ID

16.9. ROM Base Address Register

Address: 030H Index: 15 Access: Read

Bits 31:18	Rom Base address[31:18]
Bits 17:1	Rom Base address[17:1] (RO)
Bit 0	Enable Rom (RW) 1: Enable

16.10. Capability Pointer Register

Address: 034H Index: 03:00 Access: Read

Bits 31:8 reserved
Bits 7:0 *Capabilities list offset pointer (40H – Power Management)*

16.11. Interrupt Line Register

Address: 03CH Index: 03:00 Access: Read

Bits 31:16 Reserved
Bits 15:8 Interrupt Pin
01h
Bits 7:0 Interrupt Line

16.12. Power Management Capability Register

Address: 040H Index: 03:00 Access: Read

Bit 26 1= D2 support
Bit 25 1= D1 support
Bits 18:16 010 = Complies with PCI Power Management Rev 1.1
Bits 15:8 A0h = Next Capability Pointer
Bits 7:0 01h = Capability ID for PCI Power Management

16.13. Power Management Status & Control Register

Address: 044H Index: 03:00 Access: Read/Write

Bits 12:9 Data Select
Bit 8 PM enable
Bits 1:0 Ext. Power State

16.14. PCIE Capability Register

Address: 0A0H Index: 03:00 Access: Read

Bits 31:30 Reserved
Bits 29:25 Interrupt Message Number (RO, for MSI)
00001
Bit 24 Slot Implemented
Bits 23:20 Device00-03Port Type (RO)
0000: PCI Express Endpoint device (HwInit)

Bits 19:16	Capability Version (RO)
Bits 15:8	Next Capability Pointer C0h: point to MSI
Bit 7:0	Capability ID 10h (fixed at this value)

16.15. Device Capability Register

Address: 0A0H Index: 03:00 Access: Read

Bits 31:30	Reserved
Bits 29:25	Interrupt Message Number (RO, for MSI) 00001
Bit 24	Slot Implemented
Bits 23:20	Device00-03Port Type (RO) 0000: PCI Express Endpoint device (HwInit)
Bits 19:16	Capability Version (RO)
Bits 15:8	Next Capability Pointer C0h: point to MSI
Bit 7:0	Capability ID 10h (fixed at this value)

16.16. Device Control & Status Register

Address: 0A4H Index: 03:00 Access: Read

Bits 31:28	Reserved
Bits 27:26	Captured Slot Power Limit Scale (R/W by MsgD) 00: (default)
Bits 25:18	Captured Slot Power Limit Value (R/W by MsgD) 00000000: (default)
Bits 17:15	Reserved
Bit 14	Power Indicator Present (RO) 0: not implemented (fixed at this value) 1: implemented
Bit 13	Attention Indicator Present (RO) 0: not implemented (fixed at this value) 1: implemented
Bit 12	Attention Button Present (RO) 0: not implemented (fixed at this value) 1: implemented
Bits 11:9	Endpoint L1 Acceptable Latency (RO) 000: Less than 1us (fixed at this value)
Bits 8:6	Endpoint L0 Acceptable Latency (RO) 001: 64ns to less than 128ns (fixed at this value)
Bit 5	Extended Tag Field Supported (RO) 0: 5-bit Tag field supported 1: 8-bit Tag field supported (fixed at this value)

Bits 4:3	Phantom Functions Supported (RO)
	00: No function number bits used for Phantom Functions (fixed at this value);
	10: device may implement all function numbers
Bits 2:0	Max_Payload_Size Supported (RO)
	000: 128 bytes max payload size (fixed at this value)

16.17. Device Control and Status Register

Address: 0A8H Index: 03:00 Access: Read/Write

	Reserved
Bits 31:22	
Bit 21	Transactions Pending (RO)
	0: Device has issued Non-Posted Requests which have been completed
	1: Device has issued Non-Posted Requests which have not been completed
Bit 20	AUX Power Detected (RO)
	0: not detected (fixed at this value)
	1: detected
Bit 19	Unsupported Request Detected (RW1C)
	0: not detected
	1: detected (received an Unsupported Request)
Bit 18	Fatal Error Detected (RW1C)
	0: not detected
	1: detected
Bit 17	Non-Fatal Error Detected (RW1C)
	0: not detected
	1: detected
Bit 16	Correctable Error Detected (RW1C)
	0: not detected
	1: detected
Bit 15	Reserved
Bits 14:12	Max_Read_Request_Size (RW) – Maximum Read Request Size for the Device as a Requester
	000: 128 bytes max read request size
	001: 256 bytes max read request size
	010: 512 bytes max read request size (default)
	011: 1024 bytes max read request size
	100: 2048 bytes max read request size
	101: 4096 bytes max read request size
	110: Reserved
	111: Reserved
Bit 11	Enable No Snoop (RW)
	0: Enable snoop
	1: Disable snoop (default)
Bit 10	Auxiliary (AUX) Power PM Enable (RW)
Bit 9	Phantom Functions Enable (RW)
	0: Disable (fixed at this value)
	1: Enable
Bit 8	Extended Tag Field Enable (RW)
	0: Disable (default)
	1: Enable

Bits 7:5	Max_Payload_Size (RW)	000: 128 bytes max read request size (default)
		001: 256 bytes max read request size
		010: 512 bytes max read request size
		011: 1024 bytes max read request size
		100: 2048 bytes max read request size
		101: 4096 bytes max read request size
		110: Reserved
		111: Reserved
Bit 4	Enable Relaxed Ordering (RW)	0: Disable
		1: Enable (default)
Bit 3	Unsupported Request Reporting Enable (RW)	0: Disable (default)
		1: Enable
Bit 2	Fatal Error Reporting Enable (RW)	0: Disable (default)
		1: Enable
Bit 1	Non-Fatal Error Reporting Enable (RW)	0: Disable (default)
		1: Enable
Bit 0	Correctable Error Reporting Enable (RW)	0: Disable (default)
		1: Enable

16.18. Link Capabilities Register

Address: 0ACH Index: 03:00 Access: Read

Bits 31:24	Port Number (HwInit)	00000000: (fixed at this value)
	Reserved	
Bits 23:18		
Bits 17:15	L1 Exit Latency (RO)	000: Less than 1 us
		001: 1 us - 2 us
		010: 2 us - 4 us
		011: 4 us - 8 us
		100: 8 us - 16 us
		101: 16 us - 32 us(fixed at this value)
		110: 32 us - 64 us
		111: more than 64 us
Bits 14:12	L0s Exit Latency (RO)	000: Less than 64 ns
		001: 64 ns - 128 ns
		010: 128 ns - 256 ns
		011: 256 ns - 512 ns
		100: 512 ns - 1 us (fixed at this value)
		101: 1 us - 2 us
		110: 2 us - 4 us
		111: more than 4 us
Bits 11:10	Active State Power Management (ASPM) Support (RO)	00: Reserved
		01: L0s Entry Supported
		10: Reserved
		11: L0s and L1 Supported (fixed at this value)

Bits 9:4	Maximum Link Width (RO)	
	000000: Reserved	
	000001: X1	
	000010: X2	
	000100: X4	
	001000: X8	
	001100: X12	
	010000: X16 (fixed at this value)	
	100000: X32	
Bits 3:0	Maximum Link Speed (RO)	
	0001: 2.5 Gb00-03s Link (fixed at this value)	
? Address: 0A8H Index: 03:00 Access: Read/Write		
Reserved		
Bits 31:22		
Bit 21	Transactions Pending (RO)	
	0: Device has issued Non-Posted Requests which have been completed	
	1: Device has issued Non-Posted Requests which have not been completed	
Bit 20	AUX Power Detected (RO)	
	0: not detected (fixed at this value)	
	1: detected	
Bit 19	Unsupported Request Detected (RW1C)	
	0: not detected	
	1: detected (received an Unsupported Request)	
Bit 18	Fatal Error Detected (RW1C)	
	0: not detected	
	1: detected	
Bit 17	Non-Fatal Error Detected (RW1C)	
	0: not detected	
	1: detected	
Bit 16	Correctable Error Detected (RW1C)	
	0: not detected	
	1: detected	
Bit 15	Reserved	
	Max_Read_Request_Size (RW) – Maximum Read Request Size for the Device as a Requester	
Bits 14:12	000: 128 bytes max read request size	
	001: 256 bytes max read request size	
	010: 512 bytes max read request size (default)	
	011: 1024 bytes max read request size	
	100: 2048 bytes max read request size	
	101: 4096 bytes max read request size	
	110: Reserved	
	111: Reserved	
Bit 11	Enable No Snoop (RW)	
	0: Enable snoop	
	1: Disable snoop (default)	
Bit 10	Auxiliary (AUX) Power PM Enable (RW)	

Bit 9	Phantom Functions Enable (RW)	0: Disable (fixed at this value) 1: Enable
Bit 8	Extended Tag Field Enable (RW)	0: Disable (default) 1: Enable
Bits 7:5	Max_Payload_Size (RW)	000: 128 bytes max read request size (default) 001: 256 bytes max read request size 010: 512 bytes max read request size 011: 1024 bytes max read request size 100: 2048 bytes max read request size 101: 4096 bytes max read request size 110: Reserved 111: Reserved
Bit 4	Enable Relaxed Ordering (RW)	0: Disable 1: Enable (default)
Bit 3	Unsupported Request Reporting Enable (RW)	0: Disable (default) 1: Enable
Bit 2	Fatal Error Reporting Enable (RW)	0: Disable (default) 1: Enable
Bit 1	Non-Fatal Error Reporting Enable (RW)	0: Disable (default) 1: Enable
Bit 0	Correctable Error Reporting Enable (RW)	0: Disable (default) 1: Enable

16.19. Link Control Register

Address: 0B0H Index: 03:00 Access: Read

Bits 31:29	Reserved
Bit 28	Slot Clock Configuration (HwInit) 0: not uses the same physical reference clock that the platform provides 1: uses the same physical reference clock that the platform provides (fixed at this value)
Bits 27:26	Reserved
Bits 25:20	Negotiated Link Width (RO) 000001: X1 000010: X2 000100: X4 001000: X8 001100: X12 010000: X16(default) 100000: X32
Bits 19:16	Link Speed (RO) 0001: 2.5 Gb00-03s Link (fixed at this value) all others: Reserved
Bits 15:8	Reserved

Bit 7	Extended Synch (RW) 0: Disable (default) 1: Enable
Bit 6	Common Clock Configuration (RW) 0: Asynchronous clock (default) 1: Common clock
Bit 5	Retrain Link, reserved for the Endpoint, hardwired to '0'
Bit 4	Link Disable, reserved for Endpoint, hardwired to '0'
Bit 3	RCB, RO, hardwired to '0' (64B)
Bit 2	Reserved
Bits 1:0	Active State Power Management(ASPM) Control (RW) 00: Disable (default) 01: L0s Entry Enable 10: L1 Entry Enable 11: L0s and L1 Entry Enable

16.20. Message Control Register

Address: 0C0H Index: 03:00 Access: Read/Write

Bits 31:26	Reserved
Bits 25:0	MVDETPRD 3:2 Detection Previous Field Address<QW address>
Bit 2	SPFORMAT sub-picture format 1: DATAB2<7:4> for sub-picture index DATAB2<3:0> for sub-picture blending factor 0: DATAB2<7:4> for sub-picture blending factor DATAB2<3:0> for sub-picture index
Bit 1	SUBPICEN 1: sub-picture enable 0: sub-picture disable
Bit 0	ENMC 1: Motion Compensation Enable. *0: Motion Compensation disable.

16.21. Message Address Register

Address: 0C4H Index: 03:00 Access: Read/Write

Bits 31:2	Message Address
Bits 1:0	Reserved

16.22. Message Data Register

Address: 0C8H Index: 03:00 Access: Read/Write

Bits 15:0	Message Data
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16.23. PSSID Register

Address: 0D0H Index: 03:00 Access: Read/Write

Bits 2:1 SDFBSize[1:0]
Bit 0 Pssidn, SSID protection flag ('0' valid)

16.24. Local Frame Buffer Message Register1

Address: 0E0H Index: 03:00 Access: Read/Write

Bits 31:26 Local Frame Buffer Less msg[31:0] – no use

16.25. Local Frame Buffer Message Register2

Address: 0E4H Index: 03:00 Access: Read/Write

Bits 31:26 Local Frame Buffer Less msg[63:32] – no use

16.26. Advanced Error Reporting Enhanced Capability Header Register

Address: 100H Index: 03:00 Access: Read

Bits 31:20 Next Capability Offset (RO)
Bit 29 XHtEnVc1
Bit 26 XHtEnVc1
Bits 19:16 Capability Version (RO)
0001
Bits 15:0 PCI Express Extended Capability ID (RO)
0001h

16.27. Uncorrectable Error Status Register

Address: 104H Index: 03:00 Access: Read/Write

Bits 31:21 Reserved
Bit 20 Unsupported Request Error Status
ECRC Error Status
Bit 19 0: not implement
Malformed TLP Status
Bit 18 Receiver Overflow Status
Bit 17 Unexpected Completion Status
Bit 16 Completer Abort Status
Bit 15 Completion Timeout Status
Bit 14

Bit 13	Flow Control Protocol Error Status
Bit 12	Poisoned TLP Status
Bits 11:5	Reserved
Bit 4	Data Link Protocol Error Status
Bits 3:1	Reserved
Bit 0	Training Error Status
Default value = 00000000h	

16.28. Uncorrectable Error Mask Register

Address: 108H Index: 03:00 Access: Read/Write

Bits 31:21	Reserved
Bit 20	Unsupported Request Error Mask
Bit 19	ECRC Error Mask
Bit 18	Must be set to 0
Bit 17	Malformed TLP Mask
Bit 16	Receiver Overflow Mask
Bit 15	Unexpected Completion Mask
Bit 14	Completer Abort Mask
Bit 13	Completion Timeout Mask
Bit 12	Flow Control Protocol Error Mask
Bit 11	Poisoned TLP Mask
Bits 10:5	Reserved
Bit 4	Data Link Protocol Error Mask
Bits 3:1	Reserved
Bit 0	Training Error Mask
Default value = 00000000h	

16.29. Uncorrectable Error Severity Register

Address: 10CH Index: 03:00 Access: Read/Write

Bits 31:21	Reserved
Bit 20	Unsupported Request Error Severity
Bit 19	ECRC Error Severity

Bit 18	Malformed TLP Severity
Bit 17	Receiver Overflow Severity
Bit 16	Unexpected Completion Severity
Bit 15	Completer Abort Severity
Bit 14	Completion Timeout Severity
Bit 13	Flow Control Protocol Error Severity
Bit 12	Poisoned TLP Severity
Bits 11:5	Reserved
Bit 4	Data Link Protocol Error Severity
Bits 3:1	Reserved
Bit 0	Training Error Severity
	Default value = 00062011h

16.30. Correctable Error Status Register

Address: 110H Index: 03:00 Access: Read/Write

Bits 31:13	Reserved
Bit 12	Replay Timer Timeout Status
Bits 11:9	Reserved
Bit 8	REPLAY_NUM Rollover Status
Bit 7	Bad DLLP Status
Bit 6	Bad TLP Status
Bit 5:1	Reserved
Bit 0	Receiver Error Mask
	Default value = 00000000h

16.31. Correctable Error Mask Register

Address: 110H Index: 03:00 Access: Read/Write

Bits 31:13	Reserved
Bit 12	Replay Timer Timeout Mask
Bits 11:9	Reserved

Bit 8	REPLAY_NUM Rollover Mask
Bit 7	Bad DLLP Mask
Bit 6	Bad TLP Mask
Bit 5:1	Reserved
Bit 0	Receiver Error Mask
Default value = 00000000h	

16.32. Advanced Error Capabilities and Control Register

Address: 118H Index: 03:00 Access: Read/Write

Reserved	
Bits 31:9	
Bit 8	ECRC Check Enable (RWS) 0: Disable (fixed at this value) 1: Enable
Bit 7	ECRC Check Capable (RO) 0: (fixed at this value)
Bit 6	ECRC Generation Enable (RWS) 0: Disable (fixed at this value) 1: Enable
Bit 5	ECRC Generation Capable (RO) 0: (fixed at this value)
Bits 4:0	First Error Pointer (ROS) <i>Point to the first occur uncorrect</i>
Default value = 00000000h	

16.33. Header Log Register 1

Address: 11CH Index: 03:00 Access: Read/Write

Bits 31:0 *(1st DW)Header of TLP associated with error*

16.34. Header Log Register 2

Address: 120H Index: 03:00 Access: Read/Write

Bits 31:0 *(2nd DW)Header of TLP associated with error*

16.35. Header Log Register 3

Address: 124H Index: 03:00 Access: Read/Write

Bits 31:0 (3rd DW) Header of TLP associated with error

16.36. Header Log Register 4

Address: 128H Index: 03:00 Access: Read/Write

Bits 31:0 (4th DW) Header of TLP associated with error

16.37. VC Enhanced Capability Register

Address: 140H Index: 03:00 Access: Read/Write

Bits 31:20 Next Capability Offset
Bits 19:16 Capability version = 0001
Bits 15:0 PCI Express Extended Capability ID
0002h

Default value = 00010002h

16.38. Port VC Capability Register 1

Address: 144H Index: 03:00 Access: Read/Write

Bits 31:12 Reserved
Bits 11:10 Port Arbitration Table Entry Size
Reference Clock
Bits 9:8 Low Priority Extended VC Count
Bits 6:4 Reserved
Bit 3 Extended VC Count
Bits 2:0 Default value = 00000001h

16.39. Port VC Capability Register 2

Address: 148H Index: 03:00 Access: Read/Write

Bits 31:24 VC Arbitration Table Offset
Bits 23:8 Reserved
Bits 7:0 VC Arbitration Capability

Default value = 00000000h

16.40. Port VC Control & Status Register

Address: 14CH Index: 03:00 Access: Read/Write

Bits 31:17	Reserved
Bit 16	VC Arbitration Table Status
Bits 15:4	Reserved
Bit 1	VC Arbitration Select (RW) – no use
Bit 0	Load VC Arbitration Table
Default value = 00000000h	

16.41. VC0 Resource Capability Register

Address: 150H Index: 03:00 Access: Read/Write

Bits 31:24	Port Arbitration Table Offset
Bits 22:16	Maximum Time Slots
Bit 15	Reject Snoop Transactions
Bit 14	Advanced Packet Switching
Bits 13:8	Reserved
Bits 7:0	Port Arbitration Capability
Default value = 00000000h	

16.42. VC0 Resource Control Register

Address: 0C0H Index: 03:00 Access: Read/Write

Bit 31	VC Enable
Bits 30:27	Reserved
Bits 26:24	VC ID 000 for VC0
Bits 23:20	Reserved
Bits 19:17	Port Arbitration Select (RW)
Bit 16	Load Port Arbitration Table
Bits 15:8	Reserved
Bits 7:1	TC/VC Map (RW)
Bit 0	TC0/VC0 Map

Default value = 800000FFh

16.43. VC0 Resource Status Register

Address: 0C0H Index: 03:00 Access: Read

Reserved
Bits 31:18
Bit 17 VC Negotiation
Bit 16 Port Arbitration Table Status
Reserved
Bits 15:0
Default value = 00000000h

16.44. VC1 Resource Capability Register

Address: 15CH Index: 03:00 Access: Read

Port Arbitration Table Offset
Bits 31:24
Maximum Time Slots
Bits 22:16
Reject Snoop Transactions
Bit 15
Advanced Packet Switching
Bit 14
Reserved
Bits 13:8
Port Arbitration Capability
Bits 7:0
Default value = 00000000h

16.45. VC1 Resource Control Register

Address: 160H Index: 03:00 Access: Read/Write

VC Enable
Bit 31
Reserved
Bits 30:27
VC ID
Bits 26:24 001 for VC1
Reserved
Bits 23:20
Port Arbitration Select (RW)
Bits 19:17
Load Port Arbitration Table
Bit 16
Reserved
Bits 15:8
TC/VC Map (RW)
Bits 7:1
TC0/VC0 Map
Bit 0
Default value = 01000000h

16.46. VC1 Resource Status Register

Address: 164H Index: 03:00 Access: Read

Bits 31:18	Reserved
Bit 17	VC Negotiation
Bit 16	Port Arbitration Table Status
Bits 15:0	Reserved
Default value = 00000000h	

17. PCIE Configuration Registers (Base Addr. + Index)

In the register descriptions that follow, all of the reserved bits are read back as 0 unless otherwise specified.

17.1. Physical Layer Control 0

Index: 00 Access: Read/Write

Bits 7:5		XDCLpBkTimeSel<2:0>
Bit 4	XDCEnLpBkMs	
Bit 3	Reserved	
Bit 2	XDCDisScramble	
Bit 1	XDCEnL0sToRcv	
Bit 0	XDCDisCTC	

17.2. Physical Layer Control 1

Index: 01 Access: Read/Write

Bits 7:4		XDCPhyReserved<3:0>
Bit1: Link up, bit0: XDCEnTrainErr (enable link training error to be reported to the Cnfg Space reg Uncorrectable Error Status), Other bits: reserved.		
Bit 3	XDCHiDrv	
Bit 2	XDCLoDrv	
HiLo: *00:20mA, 01:10mA, 10:28mA, 11:Reserved		
Bit 1	XDCEnRxMargin	
Bit 0	XDCEnRegvalue	
Phy electrical layer control source selection.		
1:from reg b0xx, 0: from Hardware Trapping.		

17.3. Physical Layer Control 2

Index: 02 Access: Read/Write

Bits 7:0		XDCOffset<7:0>
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17.4. Physical Layer Control 3

Index: 03 Access: Read/Write

Bits 7:4		XDCDEq<3:0>
Bits 3:0		XDCDTx<3:0>

17.5. Data Link Layer Control 0

Index: 04 Access: Read

Bits 7:6	XDCRpTimeOutSel<1:0>	<i>Data Link Layer Replay Timer, counts time since last Ack/Nak received.</i> <i>X16: *00:350 Symbol Time (ST), 01:400, 10:300, 11:250;</i> <i>X8: *00:400, 01:500, 10:350, 11:300;</i> <i>X1: *00:900, 01:1000, 10:800, 11:700</i>
Bits 5:4	XDCFCusCntSel<1:0>	<i>Maximum FC update Tx frequency (if not in L0/L0s state).</i> <i>*00:26us, 01:56us, 10:86us, 11:116us.</i>
Bits 3:2	XDCFCTimerSel<1:0>	<i>FC update Tx frequency in L0/L0s state.</i> <i>X16: *00:8ST, 01:16, 10:32, 11:64;</i> <i>X8: *00:16, 01:32, 10:64, 11:128;</i> <i>X1: *00:32, 01:64, 10:128, 11:256.</i>
Bit 1	XDCRpTimeStop	<i>Enable to stop replay if received Ackd_Seq > Retry_Seq.</i>
Bit 0	XDCEnRxRetrain	<i>Enable the Link retrain initiated by Receiver not receiving any good DLLP within 200us.</i>

17.6. Data Link Layer Control 1

Index: 05 Access: Read/Write

Bits 7:5	Reserved	
Bits 4:2	XDCAckLatency<2:0>	<i>AckNak_Latency_Timer selection for Ack/Nak scheduling.</i> <i>X16: *1,2,4,8,16,64,256,1024</i> <i>X8: *2,4,8,16,32,64,256,1024</i> <i>X1: *4,8,16,32,64,128,256,1024</i>
Bit 1	XDCDisSched1Nak	<i>Discard scheduled Nak DLLP</i>
Bit 0	Reserved	

17.7. Data Link Layer Control 2

Index: 06 Access: Read/Write

Bits 7:0 XDCDLReserved<7:0>

Bit7: XDCEnTlrxNPSSingle, Ch1 single Post request processing

Bit6: XDCEnTlrxPSSingle, Ch1single NP request processing.

17.8. Transaction Layer Control 0

Index: 08 Access: Read/Write

Bit 7 XDCCDisPassVC0NP

Disable VC0 NP req pass Ch2 VFB req.

Bit 6 XDCCDisPassVC0P

Disable VC0 Post req pass Ch2 VFB req.

Bit 5 XDCEnTxFastMd

Enable transmitter in fast mode.

Bit 4 XDCEnTxInOrder

Bit 3 XDCEnPostTagNum

Enable Post TLP owns a Tag#.

Bit 2 XDCEnReq1RdRelaxOrder

Bit 1 XDCEnReq0RdRelaxOrder

Bit 0 XDCEnReq1WrRelaxOrder

17.9. Transaction Layer Control 1

Index: 09 Access: Read/Write

Bits 7:3 Reserved

Bit 2 XDCEnRxNPPassP

Bit 1 XDCEnRxPPassNP

Bit 0 XDCEnRxInOrder

17.10. Transaction Layer Control 3 (Ch0 arbitration mechanism)

Index: 0B Access: Read/Write

Bit 7 XDCEnExtPwrState (from CNFG44H bit[1:0] only)

Bits 6:5 XDCCCh0NPGntNum<1:0>

Maximum

Bit 4 XDCEnCh0Rq1PpassNP

Bit 3 XDCEnCh0Rq1NPPB2B

Bit 2	XDCEnCh0Rq1PNPB2B
Bit 1	XDCEnCh0Rq1NPSingle
Bit 0	XDCEnCh0Rq1PSingle

17.11. Channel#1 Interface 0

Index: 0C Access: Read/Write

Bits 7:6	XDCSDFBSize<1:0> *00:0MB, 01:16MB, 10:32MB, 11:64MB.
Bits 5:4	XDCSFBSIZE<1:0> *00:32MB, 01:64MB, 10:128MB, 11:256MB.
Bit 3	XDCSDFBPgSize *0: 4MB, 1: 8MB.
Bit 2	XDCEnLut8Kpage *0: 4KB, 1: 8KB.
Bit 1	XDCEnLutInLFB *0: SFB, 1: LFB.
Bit 0	XDCAperSize *0: 128MB, 1: 256MB.

17.12. Channel#1 Interface 4

Index: 10 Access: Read/Write

Bits 7:0	XDCSDFBEntry0<7:0>
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17.13. Channel#1 Interface 5

Index: 11 Access: Read/Write

Bits 7:0	XDCSDFBEntry0<15:8>
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17.14. Channel#1 Interface 5

Index: 12 Access: Read/Write

Bits 7:5	Reserved
Bits 4:0	XDCSDFBEntry0<20:16>

17.15. Channel#1 Interface 7

Index: 14 Access: Read/Write

Bits 7:0	XDCSDFBEntry1<7:0> Bit0: Entry valid flag.
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17.16. Channel#1 Interface 8

Index: 15 Access: Read/Write

Bits 7:0 XDCSDFBEntry1<15:8>

17.17. Channel#1 Interface 9

Index: 16 Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 XDCSDFBEntry1<20:16>

17.18. Channel#1 Interface 11

Index: 18 Access: Read/Write

Bits 7:0 XDCSDFBEntry2<7:0>

17.19. Channel#1 Interface 12

Index: 19 Access: Read/Write

Bits 7:0 XDCSDFBEntry2<15:8>

17.20. Channel#1 Interface 13

Index: 1A Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 XDCSDFBEntry2<20:16>

17.21. Channel#1 Interface 15

Index: 1C Access: Read/Write

Bits 7:0 XDCSDFBEntry3<7:0>

17.22. Channel#1 Interface 16

Index: 1D Access: Read/Write

Bits 7:0 XDCSDFBEntry3<15:8>

17.23. Channel#1 Interface 17

Index: 1E Access: Read/Write

Bits 7:5 Reserved

Bits 4:0 XDCSDFBEntry3<20:16>

17.24. Channel#1 Interface 19

Index: 20 Access: Read/Write

Bits 7:0 XDCSDFBEntry4<7:0>

17.25. Channel#1 Interface 20

Index: 21 Access: Read/Write

Bits 7:0 XDCSDFBEntry4<15:8>

17.26. Channel#1 Interface 21

Index: 22 Access: Read/Write

Bits 4:0 XDCSDFBEntry4<20:16>

17.27. Channel#1 Interface 23

Index: 24 Access: Read/Write

Bits 7:0 XDCSDFBEntry5<7:0>

17.28. Channel#1 Interface 24

Index: 25 Access: Read/Write

Bits 7:0 XDCSDFBEntry5<15:8>

17.29. Channel#1 Interface 25

Index: 26 Access: Read/Write

Bits 4:0 XDCSDFBEntry5<20:16>

17.30. Channel#1 Interface 28

Index: 29 Access: Read/Write

Bits 7:0 XDCSDFBEntry6<7:0>

17.31. Channel#1 Interface 29

Index: 2A Access: Read/Write

Bits 7:0 XDCSDFBEntry6<15:8>

17.32. Channel#1 Interface 31

Index: 2C Access: Read/Write

Bits 7:0 XDCSDFBEntry7<7:0>

17.33. Channel#1 Interface 32

Index: 2D Access: Read/Write

Bits 7:0 XDCSDFBEntry7<15:8>

17.34. Channel#1 Interface 33

Index: 2E Access: Read/Write

Bits 4:0 XDCSDFBEntry7<20:16>

17.35. Channel#1 Interface 35

Index: 30 Access: Read/Write

Bits 7:4 XDCSDFBLutStartAddr4<7:4>

17.36. Channel#1 Interface 36

Index: 31 Access: Read/Write

Bits 7:0 XDCSDFBLutStartAddr4<15:8>

17.37. Channel#1 Interface 37

Index: 32 Access: Read/Write

Bits 7:0 XDCSDFBLutStartAddr4<23:16>

17.38. Channel#1 Interface 38

Index: 33 Access: Read/Write

Bits 7:0 XDCSDFBLutStartAddr4<31:24>

17.39. Channel#1 Interface 39

Index: 34 Access: Read/Write

Bits 7:4 XDCPCIELutStartAddr4<7:4>

17.40. Channel#1 Interface 40

Index: 35 Access: Read/Write

Bits 7:0 XDCPCIELutStartAddr4<15:8>

17.41. Channel#1 Interface 41

Index: 36 Access: Read/Write

Bits 7:0 XDCPCIELutStartAddr4<23:16>

17.42. Channel#1 Interface 42

Index: 37 Access: Read/Write

Bits 7:0 XDCPCIELutStartAddr4<31:24>

17.43. Misc. Register 0

Index: 38 Access: Read/Write

Bits 7:5 XDCL1IdlNumSel

Link Idle time before entering into L1 state.

**000:never, 001:32ST, 010:64, 011:128,
100:256, 101:512, 110:1024, 111:2048.*

Bits 4:2 XDCL0sld1NumSel

Link Idle time before entering into L0s state.

**000:never, 001:32ST, 010:64, 011:128,*

100:256, 101:512, 110:1024, 111:2048.

Bit 1 XDCEnASPML1

Bit 0 XDCEnASPML0s

17.44. Misc. Register 1

Index: 39 Access: Read/Write

Bit 7 RGEN_NONVGAFIX

1: Enable NONVGA decode

Bit 6 RGDIS_MRDLKFIX

1: disable memory read lock

Bit 5 RGDIS_CH0WRPSRDFIX

1: disable channel 0 write pass read

Bit 4 RGDIS_GARTFIX

1: disable GART fix

Bits 3:2 Reserved

Bit 1 XDCCDisPCIEBIST

Bit 0 Reserved

17.45. Misc. Register 2

Index: 3A Access: Read/Write

Bit 7 XDCEnDebugout

Bits 6: XDCCDebugSel

17.46. Misc. Register 3

Index: 3B Access: Read/Write

Bit 7 *Reserved*

Bit 6 XDCHiVMode

Bits 5:4 XDCCR_xTermAdj<1:0>

Bits 3:2 XDCT_xTermAdj<1:0>

Bits 1:0 XDCCkTermAdj<1:0>

17.47. Misc. Register 4

Index: 3C Access: Read/Write

Bit 7	XDCEnTLCplCh0FailInt
Bit 6	XDCEnTLCplLutFailInt
Bit 5	XDCEnASPML1
Bit 4	XDCEnASPML0s
Bit 3	XDCEnTLCplMsAbortInt
Bit 2	XDCEnTLRxMsAbortInt
Bit 1	XDCEnTLTxTgAbortInt
Bit 0	XDCEnTLTxMsAbortInt

17.48. Misc. Register 5

Index: 3D Access: Read/Write

Bits 7:1	Reserved
Bit 0	XDCEnErrLutEntryInt

17.49. Misc. Register 6

Index: 3E Access: Read/Write

Write 1 for 1 PCICLK pulse

Bit 7	XClrTLCplLutFailInt
Bit 6	XClrTLCplLutFailInt
Bit 5	XClrTLCplMsAbortInt
Bit 4	XClrTLCplTgAbortInt
Bit 3	XClrTLRxTgAbortInt
Bit 2	XClrTLRxMsAbortInt
Bit 1	XClrTLTxTgAbortInt
Bit 0	XClrTLTxMsAbortInt
Read out interrupt status	
Bit 7	XTLCplLutFailInt
Bit 6	XTLCplLutFailInt

Bit 5	XTLCplMsAbortInt
Bit 4	XTLCplTgAbortInt
Bit 3	XTLRxTgAbortInt
Bit 2	XTLRxMsAbortInt
Bit 1	XTLTxTgAbortInt
Bit 0	XTLTxMsAbortInt

17.50. Misc. Register 7

Index: 3F Access: Read/Write

Write 1 for 1 PCICLK pulse

Bit 7	XDCEnSWRetrain
Bit 6	XDirtyEntireLut
Bit 5	XClrEdgeTriggerInt
Bits 4:1	Reserved

Read out interrupt status

Bits 7:1	Reserved
Bit 0	XErrLutEntryInt

17.51. Misc. Register 10

Index: 50 Access: Read/Write

Bits 3:2	MAX_READ_REQ_SIZE_H<1:0>
<i>Maximum read request length for high priority channel #2</i>	
*00: 8 x DQWORD; 01: 16 x DQWORD	
10: 32 x DQWORD; 11: 64 x DQWORD	

Bits 1:0	MAX_READ_REQ_SIZE_L<1:0>
<i>Maximum read request length for low priority channel #1</i>	
*00: 4 x DQWORD; 01: 8 x DQWORD	
10: 12 x DQWORD; 11: 16 x DQWORD	

17.52. Misc. Register 11

Index: 51 Access: Read/Write

Bit 2 REG_VFB_SNOOPN

Snooping option for high priority channel #2

*0: snooping

1: no snooping

Bits 1:0 REG_RQLIMIT<1:0>

Outstanding request limit for high priority channel #2

*00: 4 requests; 01: 8 requests

10: 16 requests; 11: 32 requests

17.53. RGRXBUSCNTR

Index: 54 Access: Read/Write

Bits 7:0 PCIE_IF/CH0 (relax arbiter) Round Robin counter

17.54. RGNRXBUSCNTR

Index: 55 Access: Read/Write

Bits 7:0 PCIE_IF/CH0 (non-relax arbiter) Round Robin counter

17.55. RGMAXNRXREQ

Index: 56 Access: Read/Write

Bits 7:4 Maximum # of outstanding non-relax request allowed

Bits 3:0 Maximum # of outstanding relax request allowed

17.56. Misc. Register 12

Index: 57 Access: Read/Write

Bit 7 GPU_NO_SNOOP_1

Bit 6 GPU_NO_SNOOP_0

Bit 5 RGDISABLE_RESET_PULSE

0: CH0 reset is a pulse, 1: CH0 reset is bit<4>.

Bit 4 RGRESETCH0

PCIE_IF/CH0 Reset. 1: Reset

Bit 3 RG_GE_HANG_AUTO_EN

Enable auto-detect GE hang-up reset protocol. 1: enable

Bit 2:0 *Reserved*

18. Power Management Registers

The PCI Power Management states are mapped as follows:

PCI PM State	Desktop Graphics	Notebook Graphics
State 0 (D0)	DPMS State 0 (Fully On)	Proprietary State 0 (Fully On)
State 1 (D1)	DPMS State 1 (Standby, Hsync Off)	Proprietary State 1 (Standby, VCLK Off)
State 2 (D2)	DPMS State 2 (Suspend, Vsync Off)	Proprietary State 2 (Suspend, both MCLK/VCLK Off)
State 3 (D3)	DPMS State 3 (Off, both Hsync/Vsync Off)	Same as State 2

18.1. Power Management Control Register

Address: 3C5 Index: 24 Access: Read/Write

- Bit 7 Select 14.3MHz Crystal Clock or 14.3/2MHz clock for the RAMDAC™ clock during RAMDAC powerdown states. 1 = Divide by 2
- Bit 6 Enable VCLK2 VCO directly without warm-up sequence (other power management registers must also be programmed)
- Bits 5:4 Divisor for 14.3MHz crystal clock input to MCLK to drive DRAM refresh cycle in power managed modes:
 - 00: 1
 - 01: 2
 - 10: 4
 - 11: 8
- Bit 3 Power Management Slow MCLK. Use the divided MCLK during standby and suspend. Active Low. Use this bit to prevent MCLK slow down or switching during standby when using external UMAcl
- Bit 2 Enable MCLK VCO directly without warm-up sequence (Other power management registers must also be programmed.). Use this bit to kill the internal MCLK VCO for external UMAclock configurations.
- Bit 1 Enable VCLK1 VCO directly without warm-up sequence (Other power management registers must also be programmed.)
- Bit 0 DAC power enable:
 - 0: off
 - 1: on
 - Reset: 4Eh

18.2. Standby Timer Control Register

Address: 3CF Index: 20 Access: Read/Write

- Bit 7 Timer initialize and enable control
 - 1: Initialize and hold standby and DPMS timer
 - 0: Enable timer
- Bits 6:4 Reserved for timer testing (read only)

Bits 3:0 Reserved
Reset: 00h

18.3. Power Management Control Register 1

Address: 3CF Index: 21 Access: Read/Write

- Bit 7 Power Management Pin Polarity for Suspend, Standby, and Pstatus pins:
 0: active high
 1: active low
- Bit 6 Enable PCI Power Management:
 0 = disable PCI PM
 1 = enable PCI PM
- Bit 5 Suspend - Chip enters suspend when this bit is set.
- Bit 4 Suspend input pin enable
- Bit 3 Enable D3 to D0 Reset
- Bit 2 Standby input pin enable
- Bit 1 Enable CLKRUN# mechanism:
 0 = disable CLKRUN# mechanism
 1 = enable CLKRUN# mechanism
- Bit 0 Enable consistent Standby and Suspend information between PCI PM and this register:
 0 = The bits within the PCI PM configuration registers will be "OR"-ed with bits [5], [3] of this register and go to the internal PM state machine.
 1 = The bits within the PCI PM configuration registers will be the same as bits [5], [3] of this register. This will allow software coherency.
- Reset: 8'h00

18.4. Power Management Control Register 2

Address: 3CF Index: 22 Access: Read/Write

- Bit 7 Test Mode for Testing Timers
 1 = Test mode for testing timers
- Bit 6 REFCLK Select:
 0: Crystal input or external clock (XMCLK) provides refresh clock during suspend.
 1: REFCLK is used as refresh clock during suspend for 64ms refresh.
If this bit is set, the suspend refresh logic ignores the suspend DRAM refresh mode bits and uses the REFCLK as the refresh clock source during suspend for 64ms refresh.
- Bits 5:4 Suspend DRAM Refresh Mode:
 00: No refresh
 01: Self-refresh
 10: Crystal osc or external clock (XMCLK) provides refresh rate for 8ms refresh.
 11: Crystal osc or external clock (XMCLK) provides refresh rate for 64ms refresh.
Bits 4-5 set the refresh mode during suspend.

- Bit 3 Disable GPIO:
 0: Allows GPIO 7-0 pins to drive data in
 1: Disables GPIO 7-0 pins (and their shared functions) from driving data. Tristates input buffers on pins, so no power is consumed if GPIO are set in input mode.
- Bit 2 Reserved
- Bit 1 Select Hardware or Software Disable Oscillator:
 0: S/W controls OSCOFF with Bit 0.
 1: H/W controls OSCOFF.
 Clearing this bit prevents the automatic oscillator shutdown without direct software control of the disable oscillator bit. Setting this bit will allow oscillator shutdown when power states are entered from hardware mechanisms.
- Bit 0 Disable Oscillator:
 0: Oscillator is allowed to function normally.
 1: Crystal oscillator is disabled.

18.5. Power Status

Address: 3CF Index: 23 Access: Read/Write

- Bit 7 Power Management Pin Polarity Bit (3CF.21.7), then chip is in Ready mode. Otherwise, it is in Standby or Suspend mode
- Bits 6:5 Chip Power Status:
 00 Ready
 01 Standby
 10 Suspend
 11 Reserved
- Bit 4 LCD Power Sequence Status:
 0: LCD Power Sequencing is not occurring at this time.
 1: LCD Power Sequencing is occurring at this time.
- Bits 3:2 Panel Power Sequencing
 00 = fast panel power sequencing
 01 = reserved
 10 = reserved
 11 = slow panel power sequencing
- Bits 1:0 DPMS VSync, Hsync:
 11: Off mode: HSync and VSync disabled. DAC LUT is full off.
 10: Suspend mode: VSync disabled. HSync active. RAMDAC™ off, contents retained.
 01: Standby mode: HSync disabled. VSync active. DAC off. LUT video data path is off. LUT I/O allowed.
 00: On mode: CRT interface is active. RAMDAC™ is full on.

Reset: XXXX0000b

19. DPMS Control Modes

19.1. DPMS Software Control Mode

In simultaneous display mode, the software control mode can be used to control DPMS low power states independent of the chip power states. In CRT display mode, S/W mode gives total DPMS control to the software. Pseudo-standby may be controlled by bits 7 and 6, as well as BLANK* timing.

19.2. DPMS Hardware Control Mode

Table 18-1 DPMS Sequence - Hardware Timer Mode

Power Level	DPMS Mode
High - Activity detected	On
Moderate - 16 min inactivity	Standby
Low - 32 min inactivity	Suspend
Lowest - 64 min inactivity	Off

DPMS hardware timer mode is defined as CRT only mode with the DPMS control mode bit set to hardware (bit 3 =1). Activity detection is set by register 3CF.21[2:0]. Status is indicated in bits 1 and 0. The timer may be controlled by S/W from 3CF.20[7].

Table 18-2 DPMS Sequence - Hardware Mode in Simultaneous Display Mode

Power Level	DPMS Mode
High - Chip on state	On
Moderate - Chip standby	Off
Low - Chip suspend	Off
Lowest - Chip off state	Off

In simultaneous display mode with hardware DPMS set, DPMS states are sequenced by the timer, pin, and register bits that control the chip power states.

19.3. Soft Power Control Register

Address: 3CF Index: 24 Access: Read/Write

- Bit 7 Enable VCLK(active High)
- Bit 6 Enable MCLK(active High)
- Bit 5 Enable CPU & DRAM data bus(active High)
- Bit 4 Reserved
- Bit 3 Under soft power control, drive ENPBLT (panel enable and / or backlight) with 0 or 1. Under hardware power control (timers, pin, register bit), this bit inverts the active polarity of ENPBLT
0 = active low
1 = active high
- Bit 2 Enable panel VDD (active High)

Bit 1 Enable panel interface signals (active High)

Bit 0 Enable panel VEE (active High)
Reset: E0h

19.4. Power Control Select Register

Address: 3CF Index: 25 Access: Read/Write

When any of 7:6, 3:0 are 1, the corresponding power control bit reads back the logic state of the internal power management engine.

Bit 7 Select soft power control for VCLK (active High)

Bit 6 Select soft power control for MCLK (active High)

Bit 5 Select soft power control for data bus (active High)

Bit 4 Select soft power control for RAMDAC™ (active High). RAMDAC™ is software enabled in 3CF.26[7:6].

Bit 3 Select soft power control for panel display enable and/or backlight (active High). See 3CF.24[4:3].

Bit 2 Select soft power control for panel VDD (active High)

Bit 1 Select soft power control for panel interface signals (active High)

Bit 0 Select soft power control for panel VEE (active High)

19.5. DPMS Control

Address: 3CF Index: 26 Access: Read/Write

Bits 7:6 Internal RAMDAC™ Power Control:
00: Normal
01: DAC off. Used when in LCD only mode
10: Standby. DAC off and LUT in low power mode. I/O allowed to LUT. May be used in LUT bypass mode.
11: Suspend: DAC off, LUT access disallowed, but contents maintained

Bits 5:4 DPMS for DVI and second CRT (share the same data path)
11: Off mode, HSYNC and VSYNC disabled
10: Suspend mode, VSYNC disabled, HSYNC active
01: Standby mode, VSYNC active, HSYNC disabled
00: On mode

Bit 3 DPMS Control:
0: Software control mode: DPMS is controlled by bits 2:1 in simultaneous display and CRT only modes.
1: Hardware control mode: DPMS is controlled by internal power states.
Software mode may be used to decouple the power modes of the CRT and LCD during simultaneous display

Bits 2:1 Reserved

Bit 0 INTEL_ALI
* The default value is 00H.

19.6. GPIO Control

Address: 3CF Index: 28-27 Access: Read/Write

Bits 15:8 GPIO Direction 7-0:
0: Read
1: Write

Bits 7:0 GPIO Data 7-0
Reset: 000000h

19.7. Reserved

Address: 3CF Index: 29 Access: Read/Write

Bits 7:0 Pulse width modulated signal for analog adjustment voltage on GPIO1:
00 = disable
Reset: 00h

Bit 0 EN_GEPWM
1: Enable GE power management.
*0: Disable GE power management.

19.8. Misc. Pin Control Register

Address: 3CFH Index: 2C Access: Read/Write

Bit 7 Reserved

Bit 6 CRT / 2nd DVI Timing Select
1: 2nd CRTC Timing.
*0: 1st CRTC Timing.

Bits 5:2 Reserved

Bit 1 Tri-state ENPVEE, ENPVDD, and ENBLIT (active LOW)

Bit 0 Reserved
Reset: 00h

19.9. Reserved

Address: 3CFH Index: 2E Access: Read/Write

Bits 7:0 Reserved

19.10. Misc. Internal Control Register

Address: 3CFH Index: 2F Access: Read/Write

- Bit 7 PCLK control:
 - 0: VGA compatible
 - 1: PCLK equals VCLK
- Bit 6 Reserved
- Bit 5 HSYNC skew control:
 - 0: one skew in graphics, two skew in text
 - 1: no skew
- Bits 4:3 Reserved
- Bit 2 Double the logical line width of the screen (active high)
- Bit 1 Text mode display FIFO prefetch cycles select:
 - 0: multiple of 8
 - 1: multiple of 4
- Bit 0 Enable display FIFO threshold control (active high); alternatively, display FIFO threshold control can be enabled by 3C0.10 bit 0.
Reset: 0000_0000h

20. Extended Mode GRAC Registers

In the descriptions that follow, all of the reserved bits are read back as 0 unless otherwise specified.

20.1. Misc. Internal Control Register

Address: 3CEH/3CFH Index: 2A Access: Read/Write

- Bit 7 Motion Video Port Suspend (active high).
 - *1: Enable Motion Video Port Suspend
 - 0: Disable Motion Video Port Suspend
- Bit 6 DVI CRTC Timing Select:
 - 1: 2nd CRTC Timing.
 - *0: 1st CRTC Timing.
- Bit 5 LCD_SEL_CTL_NEW (for DPA used in LCD logic).
 - *1: Select new fine-coarse search logic control (need to set LCD_SEL_EXT_DELYCTRL to 0)
 - 0: Original control logic would be effective
- Bit 4 LCD_SEL_EXT_DELYCTRL.
 - 1: Select external coarse code input to set coarse delay line delay
 - *0: Coarse code is controlled by internal logic
- Bit 3 REG_LCDDPARST.
 - 1: Reset DPA in LCD logic (bypass DPA in the other word)
 - *0: Normal condition
- Bit 2 LCD2DPAOFF.
 - 1: Turn off DPA for LCD logic
 - *0: Turn on DPA for LCD logic
- Bit 1 Reserved
- Bit 0 EN_GEPWM
 - 1: Enable GE power menegement
 - *0: Disable GE power menegement

20.2. Flat Panel Display Control Register

Address: 3CE/3CFH Index: 30 Access: Read/Write

- Bit 7 Enable LCD vertical shadow registers.
- Bit 6 Enable R/W shadow registers.
Reserved
- Bits 5,1 Reserved
- Bits 4,2 Reserved
- Bit 0 ENLCDHSDW
 - * The default value is 00H.

20.3. Flat Panel Attribute Enhancement

Address: 3CE/3CFH Index: 31 Access: Read/Write

- Bit 7 720 x 480 mode select.
- Bits 6:4 Number of lines per mode.
 - 111: M576
 - 110: M720 x 576
 - 101: M1200
 - 100: M720 x 480
 - 011: M1024 (1024 lines)
 - 010: M768 (768 lines)
 - 001: M600 (600 lines)
 - 000: MVGA (480 lines and less)
- Bit 3 Disable background display when hardware pop-up icon is displayed.
- Bits 2 Select alternative VSYNC., HSYNC for TFT panels.
- Bits 1:0 Reserved.

20.4. Flat Panel Reserved Register

Address: 3CE/3CFH Index: 32 Access: Read/Write

- Bits 7:4 Reserved
- Bit 3 XSRLFIX
- Bit 2:0 VDISCCKAJ_2, VDISCCKAJ_1, VDISCCKAJ_0
 - * The default value is 100.

20.5. Flat Panel Configuration Register

Address: 3CEH/3CFH Index: 33 Access: Read/Write

- Bit 7 LCD control register sync enable: To enable sync either by VSYNC or register bit (3CF.33<2>).
- Bit 6 Clock register sync enable: To enable sync either by VSYNC or register bit (3CF.33<2>).
- Bit 5 Enable CRT display (active high).
- Bit 4 Enable Flat Panel display (active high).
- Bit 3 SYNCSEL
- Bit 2 SYNCREG
- Bit 1 SYNVSHDW
- Bit 0 SYNHSHDW
 - * The default value is 00H.

20.6. Flat Panel Polarity Control Register

Address: 3CEH/3CFH Index: 34 Access: Read/Write

Bit 7	Flat panel MOD/DEN polarity control. 1: inverted *0: normal
Bit 6	Flat panel LP/PHS polarity control. 1: inverted *0: normal
Bit 5	Flat panel FLM/PVS polarity control. 1: inverted *0: normal
Bit 4	Reserved
Bit 3	Flat panel SFCLK/SCLK polarity control.. 1: inverted *0: normal
Bit 2	SFCLK_SEL. *1: SFCLK from DSTNCLK 0: SFCLK from DCLK
Bits 1:0	Reserved

20.7. Reserved

Address: 3CEH/3CFH Index: 35 Type: Read/Write

20.8. Software scratch pad 13

Address: 3CEH/3CFH Index: 36 Access: Read/Write

Bits 7:0 Software scratch pad 13.

20.9. Interrupt Status Register 1

Address: 3CEH/3CFH Index: 37 Type: Read Only

Bits 7:6	Reserved
Bit 5	DVI2 Hot Plug Detection 1: Connected 0: Disconnected
Bit 4	DVI Hot Plug Detection 1: Connected 0: Disconnected

- Bit 3 *monitor 2 sense status after anti-jitter filtering*
 1: monitor is sensed
 0: monitor is not sensed
- Bit 2 *monitor 1 sense status after anti-jitter filtering*
 1: monitor is sensed
 0: monitor is not sensed
- Bit 1 *CRT monitor 2 interrupt*
 1: interrupt
- Bit 0 *CRT monitor 1 interrupt*
 1: interrupt

20.10. Interrupt Status Register 2

Address: 3CEH/3CFH Index: 38 Access: Read Only

- Bit 7 High indicates a powered on internal DVI receiver is detected at the all of differential outputs.
- Bit 6 DVI2 interrupt.
- Bit 5 DVI interrupt.
- Bit 4 CRTC2 VSync interrupt.
- Bit 3 Motion compensation bus master interrupt.
- Bit 2 Reserved.
- Bit 1 Capture interrupt.
- Bit 0 CRTC1 VSYNC interrupt.

20.11. Interrupt Control Register 1

Address: 3CEH/3CFH Index: 39 Type: Read/Write

- Bit 7 *Current status of SROM(Read Only)*
 0: SROM is idle and write command can be issued
 1: SROM is executing write command
- Bit 6 *SROMRDSR*
 Low-high-low Sequence to read SROM status
- Bit 5 *Reserved*
- Bit 4 *DVI_HPD_PUB*
 DVI hot plug detection pin pull up, low active
 we need set this bit to 1 to disable HPD pull up.

- Bit 3 *ENDVI2INT*
Enable DVI2 Interrupt
 0: Disable
 1: Enable
- Bit 2 *CDVI2INT*
Clean DVI2 Interrupt
 0: Clean
 1: Normal
- Bit 1 *ENDVIINT*
Enable DVI Interrupt
 0: Disable
 1: Enable
- Bit 0 *CDVIINT*
Clean DVI Interrupt
 0: Clean
 1: Normal

20.12. SRAM Control

Address: 3CEH/3CFH Index: 3A Access: Read/Write

- Bit 7 Pulse to Enable SRAM write operation
- Bit 6 *Pulse to Disable SRAM write operation*
- Bit 5 Pulse to trigger bulk erase.
- Bit 4 Pulse to trigger page program.
- Bit 3 Enable Ring Oscillator function.
 1: Enable
 *0: Disable
- Bit 2 Enable pulse width modulation function.
- Bit 1 Enable clock observed output.
 1: Enable
 *0: Disable
- Bit 0 Reserved.

20.13. LVDS I2C Control

Address: 3CEH/3CFH Index: 3B Type: Read/Write (Bit 1: WO)

- Bits 7:4 Reserved

- Bit 3 LVDS_SDA_WR
1: SDA Write
*0: SDA Read
- Bit 2 Reserved.
- Bit 1 LVDS I2C SCL
* The default value is 1.
- Bit 0 LVDS I2C SDA

20.14. Interrupt Control Register 2

Address: 3CEH/3CFH Index: 3D Type: Read/Write

- Bit 7 *Enable CRTC2 VSYNC Interrupt*
- Bit 6 *Clean CRTC2 VSYNC Interrupt*
- Bit 5 *Enable CRT monitor 2 sensing interrupt*
- Bit 4 *Clean CRT monitor 2 sensing interrupt*
- Bit 3 *Enable CRT monitor 1 sensing interrupt*
- Bit 2 *Clean CRT monitor 1 sensing interrupt*
- Bit 1 Internal DVI clock edge select
*0: The falling edge of the clock is used to latch pixel data.
1: The rising edge of the clock is used to latch pixel data.
- Bit 0 Internal DVI Power Down Control
*0: All Input Pins are disabled and all differential outputs are HiZ.
1: Normal operation.

20.15. TFT Control

Address: 3CEH/3CFH Index: 3E Type: Read/Write

- Bit 7 SW_TIMER_FLAG
1: *Enable SW Timer*
*0: The Timer defined by 3CF.3F has expired
- Bit 6 Reserved
- Bit 5 Select PLL LCDCLK_90 for first view external DVI
- Bit 4 Select PLL LCKCLK for first view clock
- Bits 3:1 Reserved
- Bit 0 Reserved

20.16. Flat Panel ID Configuration Register

Address: 3CEH/3CFH Index: 41 Access: Read/Write

Bits 7:0 General purpose register from GPIO<3:0>.

20.17. TFT Panel Type Control Register

Address: 3CEH/3CFH Index: 42 Access: Read/Write

Bit 7	Enable TFT/DSTN. 1: TFT *0: DSTN
Bit 6	DUALDATA 0: Single Link 1: Dual Link
Bit 5	TFT panel type control. 0: 18-bit 1: 24-bit
Bit 3	Enable dithering (Default is 0).
Bits 4, 2:1	Reserved.
Bit 0	Select dual clock. 1: Dual shift clock selected *0: Dual shift clock un-selected

20.18. 1st DVI Control Register

Address: 3CE/3CFH Index: 43 Access: Read/Write

Bits 7:5	Reserved
Bit 4	Enable DVI Dithering 1: Enable 0: Disable
Bit 3	2 nd LCD port SFCLK polarity control. 1: Inverted 0: Normal *
Bit 2	2 nd LCD port LP polarity control. 1: Inverted 0: Normal *
Bit 1	2 nd LCD port FLM polarity control. 1: Inverted 0: Normal *
Bit 0	2 nd LCD port DE polarity control. 1: Inverted 0: Normal *

20.19. Driving Capability Control

Address: 3CE/3CFH Index: 44 Access: Read/Write

Bits 7:2	Reserved
----------	----------

- Bit 1 Vertical shadow register enable for R12, R15, R07, R09, R27.
1: Enable
0: Normal *
- Bit 0 Horizontal shadow register enable for R01, R02, R2B.
1: Enable
0: Normal *

20.20. Flat Panel Retrace Line Pulse Control

Address: 3CE/3CFH Index: 45 Access: Read/Write

- Bits 7:6 TFT VSYNC pixel adjustment
Adjust LCD VSYNC in terms of Pixel Clock
*The default value is 10
- Bits 5:3 TFTHSPIXAJ<2:0>
Adjust Hsync in terms of pixel clock
Default Value 10
- Bits 2:0 HDISPIXAJ<2:0>
Programmable pipe delay for 1st LCD port DE
000: 0 pixel clock delay; 001: 1 pixel clock delay;
010: 2 pixel clock delay; 011: 3 pixel clock delay;
*100: 4 pixel clock delay
110: 6 pixel clock delay; 111: 7 pixel clock delay;

20.21. DVI Timing Adjust

Address: 3CE/3CFH Index: 46 Access: Read/Write

- Bits 7:6 LCD2VSADJ<1:0>
Programmable pipe delay for 2nd LCD (DVI 1) port VSYNC.
*Default as 10
- Bits 5:3 LCD2HSADJ<2:0>
Programmable pipe delay for 2nd LCD port HSYNC
*Default as 10
- Bits 2:0 LCD2DEADJ<2:0>
Programmable pipe delay for 2nd LCD port DE
*Default as 100

20.22. 2nd DVI Timing Adjust

Address: 3CE/3CFH Index: 47 Access: Read/Write

- Bits 7:6 DVI2VSADJ<1:0>
Programmable pipe delay for 2nd DVI port VSYNC.
**Default as 1*
- Bits 5:3 DVI2HSADJ<2:0>
Programmable pipe delay for 2nd DVI port HSYNC
**Default as 100*
- Bits 2:0 DVI2DEADJ<2:0>
Programmable pipe delay for 2nd DVI port DE
**Default as 100*

20.23. Misc. LCD Control

Address: 3CE/3CFH Index: 48 Access: Read/Write

- Bit 7 VSYNCSEL
V sync polarity during LCD on modes
**0: positive*
1: negative
- Bit 6 HSYNCSEL
Hsync polarity during LCD on modes
**0: positive*
1: negative
- Bit 5 ENLCD2DUAL
1: Enable 2nd DVI (12 bits External)
**0: Disable 2nd DVI (12 bits External)*
- Bit 4 DVI2_DITHEN
Enable 2nd DVI Dithering.
1: Enable
**0: Disable*
- Bit 3 DVI2CKSEL
2nd DVI port CLK polarity control
1: Inverted
**0: Normal*
- Bit 2 DVI2EDGE
0: External DVI use falling edge to latch first data
1: External DVI use rising edge to latch first data

Bit 1 *Reserved*

Bit 0 DVI2DESEL
 2nd DVI port DE polarity control
 1: Inverted
 **0: Normal*

20.24. DV-DSTN Position

Address: 3CEH/3CFH Index: 49 Access: Read/Write

Bits 7:0 DV-DSTN second up position.

20.25. Scaling Engine VZF for Japanese DOS Mode

Address: 3CE/3CFH Index: 4F – 4E Access: Read/Write

Bits 15:12 Reserved.

Bits 11:0 DE_VZF_JPDOS<11:0>. The default value is 00H.

20.26. HSYNC Timing Adjust Register

Address: 3CE/3CFH Index: 50 Access: Read/Write

Bit 7 Enable refined expansion scheme.
 1: Enable
 0: Disable *

Bit 6 CENTADJ.

Bit 5 Reserved.

Bit 4 Enable reduce DE glitch.
 1: Enable
 0: Disable *

Bits 3:0 Reserved.

20.27. VSYNC Timing Adjust Register

Address: 3CE/3CFH Index: 51 Access: Read/Write

Bit 7 Sign bit for adjustment.

Bits 6:0 Adjust in terms of scan line.

20.28. Flat Panel Vertical Display Control Register

Address: 3CE/3CFH Index: 52 Access: Read/Write

Bit 7 Enable vertical centering.
 1: Enable
 0: Disable *

- Bits 6:4 Flat panel physical display resolution control. If 3CF.D1[0] ZOOMEN = 1, only panel vertical size take effect. Otherwise, both vertical and horizontal take effect.
- 111: Reserved
 - 110: Reserved
 - 101: 640 x 480
 - 100: 1400 x 1050
 - 011: 800 x 600
 - 010: 1024 x 768
 - 001: 1600 x 1200
 - 000: 1280 x 1024 *
- Bits 3:2 Select panel text mode vertical expansion scheme.
- Bit 1 Enable vertical expansion for text mode.
- 1: Enable
 - 0: Disable *
- Bit 0 Enable vertical expansion for graphic mode.
- 1: Enable
 - 0: Disable *

20.29. Horizontal Expansion/Centering Register

Address: 3CE/3CFH Index: 53 Access: Read/Write

7	6	5	4	3	2	1	0
Enable centering	Reserved	Compress text mode	Enable wide flat panel	Select wide flat panel		Horizontal expansion	Horizontal expansion

- Bit 7 Enable horizontal centering.
- 0: Disable *
 - 1: Enable
- Bit 6 Reserved.
- Bit 5 Compress text mode 9-dot font to 8-dot font.
- 0: Disable *
 - 1: Enable
- Bit 4 Enable wide flat panel.
- 0: Disable *
 - 1: Enable
- Bits 3:2 Select wide flat panel.
- 00: 1280 x 600 *
 - 01: 800 x 480
 - 10: 1024 x 600
 - 11: 1280 x 768
- Bit 1 Enable horizontal expansion for text mode.
- 0: Disable *
 - 1: Enable
- Bit 0 Enable horizontal expansion for graphic mode.
- 0: Disable *
 - 1: Enable

20.30. Video Hardware Cursor Position Control 1

Address: 3CEH/3CFH Index: 64 Access: Read/Write

Bits 7:0 Video hardware cursor X position (total 12 bits). The default value is 00H.
Note: This register setting cannot take effect until Write 3D5.43.

20.31. Video Hardware Cursor Position Control 2

Address: 3CE/3CFH Index: 65 Access: Read/Write

Bits 7:4 Video hardware cursor Y position. VHCYI<7:0> is located at 3CF.66. The default value is 0H.

Bits 3:0 Video hardware cursor X position. VHCXI<7:0> is located at 3CF.64. The default value is 0H.
Note: This register setting cannot take effect until Write 3D5.43.

20.32. Video Hardware Cursor Position Control 3

Address: 3CEH/3CFH Index: 66 Access: Read/Write

Bits 7:0 Video hardware cursor Y position (total 12 bits). The default value is 00H.
Note: This register setting cannot take effect until Write 3D5.43.

20.33. VDE Control Start Line Number

Address: 3CE/3CFH Index: 69~68 Access: Read/Write

Bits 15:0 Default=00H

20.34. VDE Control End Line Number

Address: 3CE/3CFH Index: 6B~6A Access: Read/Write

Bits 15:0 Default=00H

20.35. HDE Control Start Pixel Number

Address: 3CE/3CFH Index: 6D~6C Access: Read/Write

Bits 15:0 Default=00H

20.36. HDE Control End Pixel Number

Address: 3CE/3CFH Index: 6F~6E Access: Read/Write

Bits 15:0 Default=00H

20.37. Spread Spectrum Clock Control

Address: 3CEH/3CFH Index: 70 Access: Read/Write

Bit 7 SSC_OFF_VCK

1: Disable Spread Spectrum Control on VCK

*0: Enable Spread Spectrum Control on VCK

- Bit 6 SSC_OFF_LCK
 1: Disable Spread Spectrum Control on LCK
 *0: Enable Spread Spectrum Control on LCK
- <5>: SSC_OFF_MCK
- Bit 5 SSC_OFF_MCK
 1: Disable Spread Spectrum Control on MCK
 *0: Enable Spread Spectrum Control on MCK
- Bit 4 SSC_OFF_MCK2
 1: Disable Spread Spectrum Control on MCK2
 *0: Enable Spread Spectrum Control on MCK2
- Bits 3:0 Reserved

20.38. LVDS Control

Address: 3CE/3CFH Index: 71 Access: Read/Write

- Bit 7 HDCPI2CSEL
 2nd I2C port control by Hardware or Software
 *0: Software
 1: Hardware
- Bits 6:5 Reserved.
- Bit 4 Enable internal TMDS test mode.
 1: Enable
 0: Disable *
- Bit 3 Enable internal LVDS test mode.
 1: Enable
 0: Disable *
- Bit 2 Enable internal LVDS power.
 1: Enable
 0: Disable *
- Bit 1 Enable internal LVDS PD.
 1: Enable
 0: Disable *
- Bit 0 ENDVFLIP.
 1: Enable
 0: Disable *

20.39. Spread Spectrum Control 1

Address: 3CE/3CFH Index: 72 Access: Read/Write

- Bit 7 Power save mode for PLL.
 1: Enable
 0: Disable *

Bits 6:0 Reserved

20.40. LCDCLK Skew Control

Address: 3CE/3CFH Index: 75 Access: Read/Write

- Bit 7 Video Engine 2 software reset. The default value is 0.
- Bit 6 Video Engine 1 software reset. The default value is 0.
- Bits 5:4 LCDCLK skew control. The default value is 000.
- Bits 3:0 LCDCLK clock skew control. The default value is 000.

20.41. S/W Panel Power Sequencing Timing Control 3

Address: 3CE/3CFH Index: 76 Access: Read/Write

- Bits 7:4 Timing parameter for tVEEOFF. The default value is 0H.
- Bits 3:0 Timing parameter for tOFFBKLT. The default value is 0H.

20.42. S/W Panel Power Sequencing Timing Control 4

Address: 3CEH/3CFH Index: 77 Access: Read/Write

- Bits 7:6 DV_PBKEYSEL2<1:0>
Dual View Play back key mode function select control for surface 2(VIDEO alpha cursor, i.e. dual view alpha cursor)

- *00: W2 only
- 01: Reserved
- 10: Window key only
- 11: Video Alpha Cursor port only

- Bits 5:4 PBKEYSEL3<1:0>
Play back key mode function select control for surface 3(VGA alpha cursor, i.e. primary view alpha cursor)

- *00: VGA only
- 01: Reserved
- 10: Window key only
- 11: Alpha Cursor port only

Bits 3:0 RT7<3:0>

Timing Parameter for tPDOFF

**The default value is 0H*

20.43. External TMDS Clock Delay Control

Address: 3CE/3CFH Index: 78 Access: Read/Write

Bits 7:4 Reserved

Bits 3:0 REG_VCK_90[3:0]

External TMDS clock delay control

When chip in low speed, we need smaller delay.

When chip in high speed, we need bigger delay

**The default value is 00H*

20.44. Coarse Code Input

Address: 3CE/3CFH Index: 7A Access: Read/Write

Bits 7:2 Coarse code input to select coarse delay range. Needs to set LCD_SEL_EXT_DELYCTRL to 1 (Default value is 00000H).

Bits 1:0 Limit coarse delay line working range. Needs to set LCD_SEL_EXT_DELYCTL to 0, set LCD_SEL_CTL_NEW to 1.

20.45. I/O Pads Driving Strength Control

Address: 3CEH/3CFH Index: 7B Access: Read/Write

Bits 7:0 PDNSEL_P2, PDPSEL_P2 (TV or 2nd LCD). The default value is 88H.

20.46. VCK_90 Skew Control

Address: 3CE/3CFH Index: 7C Access: Read/Write

Bits 7:4 Reserved.

Bits 3:0 REG_VCK_90. The default value is 08H.

20.47. Scaling Engine Vertical Zoom Factor Accumulator Initial Parameter

Address: 3CE/3CFH Index: 7D Access: Read/Write

Bit 7 Reserved.

Bits 6:2 The initial VZF accumulator value which is used to balance the BETA of the last line.

Bits 1:0 Reserved.

20.48. Scaling Engine Horizontal Zoom Factor Accumulator Initial Parameter

Address: 3CE/3CFH Index: 7E Access: Read/Write

- Bit 7 Reserved.
- Bits 6:2 The initial HZF accumulator value which is used to balance the ALPHA of the last pixel.
- Bits 1:0 Reserved.

20.49. Misc. Window2 Control

Address: 3CEH/3CFH Index: 81 Access: ReadWrite

- Bit 7 Window2 STADD latch
 - 1: enable
 - *0: disable
- Bits 6:1 Reserved
- Bit 0 ENVIDEO2
 - 1: Window2 enable
 - *0: Window2 disable

21. DVD Video Registers

Volari XP10 implements XGI's THAMA™ architecture for DVD playback. It integrates on-chip motion compensation hardware for accelerating MPEG-2 video decoding.

The software components of the THAMA™ architecture consist of two parts, client software and HAL driver.

Client software which takes care of AC-3 decoding, as well as MPEG-2 video decoding up to the output of the IDCT HAL driver, which controls the hardware directly

The client software and HAL driver communicate through DirectDraw™ surfaces. The HAL driver provided by XGI controls all DVD video decoding and display operations supported by the Volari XP10.

The Volari XP10 supports Macrovision™ 7.01, as required for compliance with DVD specifications.

Y0 reference Address Register Port: 2250~2252 Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	Y0-reference start address (QWORD)

Y1-reference Address Register Port: 2254~2256, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	Y1-reference start address (QWORD)

Y2-reference Address Register Port: 2258~225A, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	Y2-reference start address (QWORD)

Y3-reference Address Register Port: 225c~225E, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	Y3-reference start address (QWORD)

Y4-reference Address Register Port: 2210~2212 Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	Y4-reference start address (QWORD)

Y5-reference Address Register Port: 2214~2216, Type: R/W

Bit	Description
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[31:24]	Reserved
[23:0]	Y5-reference start address (QWORD)

Y6-reference Address Register Port: 2218~221a, Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	Y6-reference start address (QWORD)

Y7-reference Address Register Port: 221c~221e, Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	Y7-reference start address (QWORD)

U0-reference Address Register Port: 2260~2262 Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	U0-reference start address (QWORD)

U1-reference Address Register Port: 2264~2266, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	U1-reference start address (QWORD)

U2-reference Address Register Port: 2268~226A, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	U2-reference start address (QWORD)

U3-reference Address Register Port: 226c~226E, Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	U3-reference start address (QWORD)

U4-reference Address Register Port: 2220~2222 Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	U4-reference start address (QWORD)

U5-reference Address Register Port: 2224~2226, Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	U5-reference start address (QWORD)

U6-reference Address Register**Port: 2228~222a, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	U6-reference start address (QWORD)

U7-reference Address Register**Port: 222c~222e, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	U7-reference start address (QWORD)

V0-reference Address Register**Port: 2270~2272 Type: R/W**

Bit	Description
[23:22]	Reserved
[21:0]	V0-reference start address (QWORD)

V1-reference Address Register**Port: 2274~2276, Type: R/W**

Bit	Description
[23:22]	Reserved
[21:0]	V1-reference start address (QWORD)

V2-reference Address Register**Port: 2278~227A, Type: R/W**

Bit	Description
[23:22]	Reserved
[21:0]	V2-reference start address (QWORD)

V3-reference Address Register**Port: 227c~227E, Type: R/W**

Bit	Description
[23:22]	Reserved
[21:0]	V3-reference start address (QWORD)

V4-reference Address Register**Port: 2230~2232 Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V4-reference start address (QWORD)

V5-reference Address Register**Port: 2234~2236, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V5-reference start address (QWORD)

V6-reference Address Register**Port: 2238~223a, Type: R/W**

Bit	Description
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[31:24]	Reserved
[23:0]	V6-reference start address (QWORD)

V7-reference Address Register **Port: 223c~223e, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V7-reference start address (QWORD)

IDCT_WDAT_REG **Port: 2240~2243 Type: R/W**

Bit	Description
[31:0]	IDCT Debug Data In

ZZINDEX **Port: 2244~2247 Type: R/W**

Bit	Description
[31:0]	ZZ Debug Index

ZZW_DATA **Port: 2248~224b Type: R/W**

Bit	Description
[31:0]	ZZ Debug Data

Y0 reference Address Register **Port: 2250~2252 Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	Y0-reference start address (QWORD)

Y1-reference Address Register **Port: 2254~2256, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	Y1-reference start address (QWORD)

Y2-reference Address Register **Port: 2258~225a, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	Y2-reference start address (QWORD)

Y3-reference Address Register **Port: 225c~225e, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	Y3-reference start address (QWORD)

U0-reference Address Register **Port: 2260~2262 Type: R/W**

Bit	Description
[31:24]	Reserved

[23:0]	U0-reference start address (QWORD)
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U1-reference Address Register **Port: 2264~2266, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	U1-reference start address (QWORD)

U2-reference Address Register **Port: 2268~226a, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	U2-reference start address (QWORD)

U3-reference Address Register **Port: 226c~226e, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	U3-reference start address (QWORD)

V0-reference Address Register **Port: 2270~2272 Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V0-reference start address (QWORD)

V1-reference Address Register **Port: 2274~2276, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V1-reference start address (QWORD)

V2-reference Address Register **Port: 2278~227a, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V2-reference start address (QWORD)

V3-reference Address Register **Port: 227c~227e, Type: R/W**

Bit	Description
[31:24]	Reserved
[23:0]	V3-reference start address (QWORD)

MC ID Register **Port: 2280** **Type: RO**

Bit	Description
[7:0]	MC Version ID, Read only 10h: Ferrari

MC Control Register Port: 2281 Type: R/W

Bit	Description
[7:4]	Local MC read length. (only if bit3 = 1)
[6:4]	Reserved
[3]	Enable local MC read length control. Driver need to check the maximum read length allowed by PCIE.
[2]	Reset PCIE CH2 MC
[1]	Reset PCIE CH2 MC FIFO counter.
[0]	MC mode: 1: Enable 0: Disable

MC Frame Buffer Control Register Port: 2282 Type: R/W

Bit	Description
[7]	Interlaced display
[6]	Bypass TV flicker filter: 0: use TV CRTC 1: use VGA CRTC
[5]	Separate Display and Decode Command 0: combine display and decode 1: separate display and decode
[4]	IDCT Function Enable 0: Motion Compensation Function only 1: Motion Compensation and IDCT Function
[3]	Surface Type 0: MVCA Surface 1: YUV Planner mode (YV12 mode)
[2]	NV12 Mode 1: NV12 Mode Enable
[1:0]	FB configuration, reserved at 00

MC Control Register - Additional Port: 2283 Type: R/W

Bit	Description
[7:6]	Reserved
[5]	MC PCIE channel goes through order request queue enable.
[4:2]	reserved
[1]	8-Frame Mode Enable. 1: Enable
[0]	Separate Command and Data. 1: Separate CMD & DATA Enable 0: disable

MC Command Queue Register 1st DW Port: 2284~2287, Type: WO

Bit	Description
[31:12]	PCI: Page table address AGP: Bit-stream buffer address, always aligned at 4K-page head.
[11]	MC Buffer1: 1: High Target Buffer. “ {[11],[3:2]} = 100: F4, 101: F5, 110: F6, 111: F7 ”
[10:9]	Video output display fields: (Combine Display / Decode) 00: Reserved 01: top 10: bottom 11: both
[8:6]	Video output display buffer: (Combine Display / Decode) 000: F0; 001: F1; 010: F2; 011: F3, 100: F4, 101: F5, 110: F6, 111: F7.
[5:4]	MC output decode fields: 00: Reserved 01: top 10: bottom 11: both
[3:2]	MC Buffer1: 00:F0, 01: F1, 10: F2, 11: F3
[1]	IDCT Format: 1: 8-bit IDCT 0: 16-bit IDCT
[0]	MC Command Type 0: Display Only 1: Display & Decode

MC Command Queue Register 2nd DW Port: 2284~2287, Type: WO

Bit	Description
[31:23]	Reserved
[22:0]	AGP Bit-Stream Length (DW)

MC Status Register Port: 2284~2287, Type: RO

Bit	Description
[31:30]	Reserved
[29:25]	Data Queue Status
[24]	CMD Content-Additional, Target MC-Buffer F4-F7
[23:18]	Display Queue Status
[17]	MC Done Interrupt
[16]	MC Pop-Out Interrupt
[15:11]	Command Queue Status
[10:1]	MC Decode Command Content
[0]	MC Busy

MVCA Y-reference Address Register Port: 2288, 2289, 228A Type: R/W

Bit	Description
-----	-------------

[31:24]	Reserved
[23:0]	Y-reference start address (QWORD)

MVCA U-reference Address Register Port: 228C, 228D, 228E Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	U-reference start address (QWORD)

MVCA V-reference Address Register Port: 2290, 2291, 2292 Type: R/W

Bit	Description
[31:24]	Reserved
[23:0]	V reference start address (QWORD)

MC Display Y-Address Offset Register Port: 2294, 2295, 2296 Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	Y address offset of first display pixel from first pixel (top left hand corner) of picture (QWORD)

MC Display U-Address Offset Register Port: 2298, 2299, 229A Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	U address offset of first display pixel from first pixel (top left hand corner) of picture (QWORD)

MC Display V-Address Offset Register Port: 229C, 229D, 229E Type: R/W

Bit	Description
[23:22]	Reserved
[21:0]	V address offset of first display pixel from first pixel (top left hand corner) of picture (QWORD)

MC Horizontal Macroblock Count Register Port: 22A0 Type: R/W

Bit	Description
[7:0]	Number of horizontal macroblocks

MC Vertical Macroblock Count Register Port: 22A2 Type: R/W

Bit	Description
[7:0]	Number of vertical macroblocks

MVCA Frame Buffer Y-Length Register Port: 22A4, 22A5 Type: R/W

Bit	Description
[23:19]	Reserved
[18:0]	Number of QWORD in a Y frame

MC Y Buffer Stride Register Port: 22A8 Type: R/W

Bit	Description
[7:0]	Stride size of Y buffer, 128-bit aligned

MC U/V Buffer Stride Register Port: 22A9 Type: R/W

Bit	Description
[7:0]	Stride size of U/V buffer, 128-bit aligned

MC Display Queue Register Port: 22AC~22AF, Type: WO

Bit	Description
[31:11]	Reserved
[10:9]	Video output display fields: (Combine Display / Decode) 00: Reserved 01: top 10: bottom 11: both
[8:6]	Video output display buffer: (Combine Display / Decode) 000: F0; 001: F1; 010: F2; 011: F3; Other: Reserved
[5:0]	Reserved

MC Debug Index Register Port: 22B0 Type: R/W

Bit	Description
[7:0]	Debug Index 0x01 ~ 0x0d: MC Debug 0x0e : ZZ Debug 0x0f ~ 0x12: IDCT Debug

Debug Address for FIFO Register Port: 22B1, Type: R/W

Bit	Description
[7:0]	Debug Address for FIFO

IDCT Debug Index Register Port: 22B2, Type: R/W

Bit	Description
[7:0]	IDCT Debug Index

MC Debug Data Register Port: 22B4, 22B5, 22B6, 22B7 Type: RO

Bit	Description
-----	-------------

[31:0]	Debug Data output bus
--------	-----------------------

Clear MC Done Interrupt Port: 22B8 Type: WO

Bit	Description
[7:0]	One write command will clear MC done interrupt

Clear MC Pop-out Interrupt Port: 22B9 Type: WO

Bit	Description
[7:0]	One write command will clear MC Pop-out Interrupt

MC Data Queue Register 1st DW Port: 22BC~22BF, Type: WO

Bit	Description
[31:12]	Page Table Address / Bit-Stream Address (4K Aligned)
[11]	2 nd Data Queue 1: I-Block 8-bit mode 0: I-Block 16-bit mode
[10:0]	Reserved

MC Data Queue Register 2nd DW Port: 22BC~22BF, Type: WO

Bit	Description
[31:23]	Reserved
[22:0]	AGP Bit-Stream Length (DW)

FRONT PARSER DEBUG INDEX Port: 22C0~22C3 Type: R/W

Bit	Description
[31:0]	Front Parser Debug Index

FRONT PARSER DEBUG WRITE DATA Port: 22C4~22C7 Type: R/W

Bit	Description
[31:0]	Front Parser Debug Write Data

Movie Detection Status Port: 22E3~22E0 Type: R/W

Bit	Description
[31]	Set 1 to signal the H/W that the movie detection registers are all ready for H/W to use. H/W clear this bit when movie detection job has been done.
[21]	Movie mode to display
[20]	Progressive
[19]	Movie Parity
[17:0]	Field Motion

Frame Motion Port: 22E7~22E4 Type: R/W

Bit	Description
-----	-------------

[31:0]	
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22. Digital TV Encoder Interface

22.1. TV Output Vertical Scaling Control Register

Address: 3D4H/3D5H Index: C6 Access: Read/Write

- Bit 7 TV display vertical scaling.
1: Enable scaling when 3D5.C1.bit6 = 1
*0: Normal condition
- Bit 6 TV display vertical scaling direction.
1: Scaled down
*0: Scaled up
- Bit 5 TV display hardware cursor control when vertical scaled down is selected.
1: Hardware cursor is compressed proportionally
*0: Normal condition
- Bit 4 TV display vertical scaled down algorithm.
1: Filtered
*0: Drop line
- Bit 3 TV display vertical scaled up algorithm.
1: Average line for better quality
*0: Replicate line
- Bit 2 Hardware cursor compression test.
1: Enable testing mode
*0: Normal mode
- Bit 1 Reserved
- Bit 0 Reserved

22.2. Software Scratch Pad 11 - 8

Address: 3D4H/3D5H Index: CB – C8 Access: Read/Write

22.3. Digital TV Master Mode Control 0

Address: 3D4H/3D5H Index: D0 Access: Read/Write

- Bits 7:0 EQUAEND (HDLOAD)
Initial Value [7:0] of HDE start from rising/falling edge of HSYNC. The starting point is depending on SYNC polarity select register(3D5.D1<5:4>)

22.4. Digital TV Master Mode Control 1

Address: 3D4/3D5H Index: D1 Access: Read/Write

- Bit 7 ENDTVMOD
0: Disable *
1: Enable

- Bit 6 ENHVDLOAD
0: Disable *
1: Enable
- Bit 5 HSYNC polarity select.
0: High active *
1: Low active
- Bit 4 VSYNC polarity select.
0: High active *
1: Low active
- Bit 3 TV master mode.
0: Disable *
1: Enable
- Bit 2 Enable Digital TV.
0: Disable *
1: Enable
- Bit 1 ENDTVMOD1
0: Disable *
1: Enable
- Bit 0 EQUAEND<8> (HDL0AD<8>).
Initial value [8] of HDE start from rising/falling edge of HSYNC.

22.5. Digital TV Master Mode Control 2

Address: 3D4H/3D5H Index: D2 Access: Read/Write

- Bits 7:0 VDHLOAD
Initial Value [7:0] of VDE start from rising/falling edge of VSYNC. The starting point is depending on SYNC polarity select register(3D5.D1<5:4>).

22.6. Digital TV Master Mode Control 3

Address: 3D4H/3D5H Index: D3 Access: Read/Write

- Bits 7:4 Reserved
- Bits 3:0 Initial value [11:8] of VDE start from rising/falling edge of VSYNC.

22.7. TV Control

Address: 3D4H/3D5H Index: D6 Access: Read/Write

- Bits 7:5 Reserved.
- Bit 4 EXTTVVSIEN(obsolete)
1: Enable TV VSYNC input buffer
*0: Enable TV VSYNC output buffer.

- Bit 3 EXTTVHSIEN(obsolete)
 1: Enable TV HSYNC input buffer
 *0: Enable TV HSYNC output buffer.
- Bit 2 Enable second view play TV.
- Bit 1 Bypass TVX2 PLL.
- Bit 0 Enable external TV.

22.8. Internal TVX2 Control

Address: 3D4H/3D5H Index: D7 Access: Read/Write

- Bit 7 TVX2 DAC is used as CRT2 DAC.
- Bit 6 When DVI uses TVX2 DAC, this bit controls DAC to turn off.
- Bit 5 Suspend TVX2.
- Bit 4 TVREGSTOP
 After programming TVX2, issue a pulse of TVREGSTOP
- Bits 3:0 Software DELAY_RPO control for TVX2 clock source.

22.9. Digital TV Control Register

Address: 3C5 Index: D8 Access: Read/Write

- Bit 7 REG_VVDE
 issue test VVDE for simulation.
- Bits 6:4 REG_TCLK[2:0]
 half TCLK(FLAGD) phase control
 xx0: phase of half TCLK is not controlled
 x01: falling edge of half TCLK is aligned to rising edge of HS.
 x11: rising edge of half TCLK is aligned to rising edge of HS.
 Normally, we set it to 011.
- Bit 3 TV signature enable
 a rising edge of this signal will trigger a signature testing.
- Bit 2 TV signature scheme
 0: test signature all the time
 1: test signature for DE only

Bits 1:0 select which 16 bit of 48 bits signature is read out by register 3d5.db ~ 3d5.da
00: signature[15:0]
01: signature[31: 16]
10: signature[47: 32]
11: reserved

22.10. Digital TV Signature Status Register

Address: 3C5 Index: D9 Access: Read Only

Bit 7 signature ready
1: signature is ready to read
0: signature is not ready or signature is not enabled at all
Bits 6:0 Reserved

22.11. Digital TV Signature Data Register

Address: 3C5 Index: DB~DA Access: Read Only

Bits 15:0 TV Signature data

22.12. TV Horizontal Total Shadow Register

Address: 3D4H/3D5H Index: E0 Access: Read/Write

22.13. TV End Horizontal Blanking Shadow Register

Address: 3D4H/3D5H Index: E3 Access: Read/Write

22.14. TV Start Horizontal Retrace Pulse Shadow Register

Address: 3D4H/3D5H Index: E4 Access: Read/Write

22.15. TV End Horizontal Retrace Shadow Register

Address: 3D4H/3D5H Index: E5 Access: Read/Write

22.16. TV Vertical Total Shadow Register

Address: 3D4H/3D5H Index: E6 Access: Read/Write

22.17. TV CRT Controller Overflow Shadow Register

Address: 3D4H/3D5H Index: E7 Access: Read/Write

22.18. TV Vertical Retrace Start Shadow Register

Address: 3D4H/3D5H Index: F0 Access: Read/Write

22.19. TV Vertical Retrace End Shadow Register

Address: 3D4H/3D5H Index: F1 Access: Read/Write

22.20. TV End Vertical Blanking Shadow Register

Address: 3D4H/3D5H Index: F6 Access: Read/Write

22.21. TVX2 Register Address

Address: 3D4H/3D5H Index: FE Access: Read/Write

Bits 7:0 TVX2 register address

22.22. TVX2 Register Data

Address: 3D4H/3D5H Index: FF Access: Read/Write

Bits 7:0 <7:0> TVX2 register data
when read, first write address to 3d5.fe, then read data from 3d5.ff.
when write, first write address to 3d5.fe, then write data to 3d5.ff

After finish programming TVX2, issue a pulse of STOP by toggling 3d5.d7[4].

23. Display Engine

The Volari XP10 's Display Engine brings the high performance overlay platform and high quality of display image. It has the capability of displaying images on multiple display devices simultaneously. These devices can be CRT, TV, DVI, and/or LCD panel.

- Programmable Register Description

FORMATTER

Address	Register Name	Attribute	Size
3C5.7B[2]	DISLVL	R/W	1-bit
3C5.57	PBKEYSEL	R/W	8-bit
3CF.DC	CALPHA1	R/W	8-bit
3CF.DB[0]	ALPHAEN1	R/W	1-bit
3CF.DB[1]	CALPHAEN1	R/W	1-bit
3D5.BF[2:0]	CMD	R/W	3-bit
3CF.DE, 3D5.BB-BA	KEYDATAL	R/W	24-bit
3CF.DF 3D5.BD-BC	KEYDATAH	R/W	24-bit
3C5.BD[6]	MC4	R/W	1-bit
3CF.DB[2]	SKEYPOL1	R/W	1-bit
3CF.62[2]	ENCOLORKEY1	R/W	1-bit
3CF.62[0]	ENFOVERLAY1	R/W	1-bit
3CF.67	PBKEYSEL2	R/W	8-bit
3CF.DD	CALPHA2	R/W	8-bit
3CF.DB[4]	ALPHAEN2	R/W	1-bit
3CF.DB[5]	CALPHAEN2	R/W	1-bit
3D5.BF[6:4]	HCMD	R/W	3-bit
3CF.6D-6B	KEYDATAL2	R/W	24-bit
3CF.E2-E0	KEYDATAH2	R/W	24-bit
3C5.BD[7]	MC5	R/W	1-bit
3CF.DB[6]	SKEYPOL2	R/W	1-bit
3CF.62[3]	ENCOLORKEY2	R/W	1-bit
3CF.62[1]	ENFOVERLAY2	R/W	1-bit

BLENDER

Address	Register Name	Attribute	Size
3CF.DB[3]	S1_PREMUT1	R/W	1-bit
3CF.BD[7]	S2_PREMUT1	R/W	1-bit

CONVERTER

Address	Register Name	Attribute	Size
3CF.DA[2:0] 3CF.D9	PITCH	R/W	11-bit
3CF.DA[7:6]	BAND128X32 (01)	R/W	1-bit

3CF.DA[7:6]	BAND64X64 (10)	R/W	1-bit
3CF.DA[7:6]	BAND32X128 (11)	R/W	1-bit
3D5.38[3]	TRCOLOR	R/W	1-bit
*3CF.48[2:0] 3CF.47	S1PITCH	R/W	11-bit
3CF.D3[6:5]	S1BAND128X32 (01)	R/W	1-bit
3CF.D3[6:5]	S1BAND64X64 (10)	R/W	1-bit
3CF.D3[6:5]	S1BAND32X128 (11)	R/W	1-bit

Multiple Display

Address	Register Name	Attribute	Size
3C5.BE[3]	DVEN	R/W	1-bit
3CF.2A[6]	LCD2DVEN	R/W	1-bit
3CF.2C[1]	TRIP1F1N	R/W	1-bit
3CF.2C[2]	TRIP1F2N	R/W	1-bit
3CF.31[6:4]	VGA mode MXXX	R/W	3-bit
3CF.33[4]	LCD	R/W	1-bit
3CF.33[5]	CRT	R/W	1-bit
3CF.42[6]	DUALDATA	R/W	1-bit
3CF.42[7]	TFT	R/W	1-bit
3CF.52[6:4]	LCD panel size PXXX	R/W	3-bit
3CF.53[[3:2]	LCD wide panel size HX_X	R/W	2-bit
3CF.71[1]	ENLVDS PD	R/W	1-bit
3CF.71[2]	ENLVDS PWR	R/W	1-bit
3CF.75[1]	PD_TMDS	R/W	1-bit
3C5.7E[4]	NEWREG4VEO_12	R/W	1-bit
3C5.7E[5]	NEWREG4VEO_13	R/W	1-bit
3D5.D1[2]	ENDTV	R/W	1-bit
3D5.D1[3]	ENTVMA	R/W	1-bit
3C5.DC[1:0]	LUTXRDEN	R/W	2-bit
3C5.DC[2]	LUT2WRENB	R/W	1-bit
3C5.DD[4]	LUT0WREN	R/W	1-bit
3C5.DD[6]	LUT1WRENB	R/W	1-bit
3CF.D1[3]	LUT1BYPASS	R/W	1-bit
3CF.D1[0]	ZOOMEN	R/W	1-bit
3CF.D1[1]	SELVQ0	R/W	1-bit
3CF.D5[6]	VCEN_BYPASS	R/W	1-bit
3CF.52[7][1:0]	VCENEXP	R/W	3-bit
3CF.53[7][1:0]	HCENEXP	R/W	3-bit
3CF.D3[7]	ENHINTE	R/W	1-bit
3CF.D3[2:0], 3CF.D2	DE_HZF[11:0]	R/W	11-bit
3CF.D5[7]	ENVINTE	R/W	1-bit
3CF.D5[2:0], 3CF.D4	DE_VZF[11:0]	R/W	11-bit

23.1. Display Engine Control 1

Address: 3CE/3CFH Index: D1 Access: Read/Write

- | | |
|-------|---|
| Bit 7 | Enable DISPQ64 read burst.
0: Disable *
1: Enable |
| Bit 6 | Enable downgrade horizontal expansion for 1280x600 panel.
Ex. 640 -> 1280 => 960
720 -> 1080 => 900
800 -> 1200 => 1000
0: Disable *
1: Enable |
| Bit 5 | Scaling engine BIST testing result (Read-Only).
0: Pass *
1: Defective |
| Bit 4 | Enable scaling engine BIST testing.
0: Disable *
1: Enable |
| Bit 3 | Enable bypass LUT1.
0: Disable *
1: Enable |
| Bit 2 | DISPQ 32/64 level select.
0: 32 level *
1: 64 level |
| Bit 1 | Internal CRTC Q counter select.
0: Select Q1 as CRTC counter *
1: Select Q0 as CRTC counter |
| Bit 0 | Enable new scaling engine.
0: Disable *
1: Enable |

23.2. New Scaling Engine Horizontal Zoom Factor

Address: 3CEH/3CFH Index: D2 Access: Read/Write

- Bits 7:0 Scaling engine horizontal zoom factor (total 11 bits). The default value is 00H.

23.3. Scaling Engine Control

Address: 3CEH/3CFH Index: D3 Access: Read/Write

- | | |
|-------|--|
| Bit 7 | Enable scaling engine horizontal interpolation.
1: Enable
0: Disable * |
|-------|--|

- Bits 6:5 Surface1 band mode control.
 11: Surface1 band 32x128
 10: Surface1 band 64x64
 01: Surface1 band 128x32
 00: Disable surface1 bandmode *
- Bit 4 Enable Hardware Vertical Zoom Factor Adjustment for Japanese DOS mode.
 1: Enable
 0: Disable *
- Bits 3:0 Scaling engine horizontal zoom factor (total 12 bits). DE_HZF<7:0> is located at 3CF.D2.
 * The default value is 00H.

23.4. **Scaling Engine Vertical Zoom Factor**

Address: 3CEH/3CFH Index: D4 Access: Read/Write

- Bits 7:0 Scaling engine vertical zoom factor (total 11 bits). The default value is 00H.

23.5. **Scaling Engine Control 2**

Address: 3CEH/3CFH Index: D5 Access: Read/Write

- Bit 7 Enable scaling engine vertical interpolation.
 1: Enable
 0: Disable *
- Bit 6 Vertical DE select.
 1: Bypass vertical centering and select CRT VDE
 0: Select VCENTER's VDE *
- Bit 5 Bypass scaling engine.
 1: Enable
 0: Disable *
- Bit 4 Reserved.
- Bits 3:0 Scaling engine vertical zoom factor (total 12 bits). DE_VZF<7:0> is located at 3CF.D4.
 * The default value is 00H.

23.6. **VGA Blue Sharp Parameter**

Address: 3CEH/3CFH Index: D6 Access: Read/Write

- Bits 7:0 SHARP_PAR_B<7:0>. The default value is 00H.

23.7. **VGA Green Sharp Parameter**

Address: 3CEH/3CFH Index: D7 Access: Read/Write

- Bits 7:0 SHARP_PAR_G<7:0>. The default value is 00H.

23.8. **VGA Red Sharp Parameter**

Address: 3CEH/3CFH Index: D8 Access: Read/Write

Bits 7:0 SHARP_PAR_R<7:0>. The default value is 00H.

23.9. Surface 0 Band Mode Pitch 1

Address: 3CEH/3CFH Index: D9 Access: Read/Write

Bits 7:0 Surface 0 band mode pitch (total 11 bits). The default value is 00H.

23.10. Surface 0 Band Mode Control

Address: 3CEH/3CFH Index: DA Access: Read/Write

Bits 7:6 Surface0 band mode control.
11: Surface1 band 32x128
10: Surface1 band 64x64
01: Surface1 band 128x32
00: Disable surface0 bandmode *

Bit 5 Enable CPU R/W band mode.
1: Enable
0: Disable *

Bit 4 Disable MCK for display engine in order to save power.
1: Disable
0: Enable *

Bit 3 Reserved.

Bits 2:0 Surface 0 band mode pitch (total 11 bits). PITCH<7:0> is located at 3CF.D9.
* The default value is 0H.

23.11. Display Engine Control 3

Address: 3CE/3CFH Index: DB Access: Read/Write

Bit 7 Enable surface 2 alpha pre-multiplied.
0: Disable *
1: Enable

Bit 6 Surface 2 source key polarity.
0: Kill while surface 2 source color inside range *
1: Keep while surface 2 source color inside range

Bit 5 Enable surface 2 constant alpha blending.
0: Disable *
1: Enable

Bit 4 Enable surface 2 pixel-by-pixel alpha blending.
0: Disable *
1: Enable

Bit 3 Enable surface 1 alpha pre-multiplied.
0: Disable *
1: Enable

- Bit 2 Surface 1 source key polarity.
0: Kill while surface 1 source color inside range *
1: Keep while surface 1 source color inside range
- Bit 1 Enable surface 1 constant alpha blending.
0: Disable *
1: Enable
- Bit 0 Enable surface 2 pixel-by-pixel alpha blending.
0: Disable *
1: Enable

23.12. Surface 1 Constant Alpha

Address: 3CEH/3CFH Index: DC Access: Read/Write

Bits 7:0 CALPHA1<7:0>. The default value is 00H.

23.13. Surface 2 Constant Alpha

Address: 3CEH/3CFH Index: DD Access: Read/Write

Bits 7:0 CALPHA1<7:0>. The default value is 00H.

23.14. Surface 1 Source Key Lower Bound

Address: 3CEH/3CFH Index: DE Access: Read/Write

Bits 7:0 Surface 1 Source (Chroma) Key Lower Bound (Total 24 bits). KEYDATAL<15:0> is located at 3D5.BB ~ 3D5.BA.
* The default value is 00H.

23.15. Surface 1 Source Key Upper Bound

Address: 3CEH/3CFH Index: DF Access: Read/Write

Bits 7:0 Surface 1 Source (Chroma) Key Upper Bound (Total 24 bits). KEYDATAH<15:0> is located at 3D5.BD ~ 3D5.BC.
* The default value is 00H.

23.16. Surface 2 Source Key Upper Bound

Address: 3CEH/3CFH Index: E2 – E0 Access: Read/Write

Bits 23:0 Surface 2 Source (Chroma) Key Upper Bound (Total 24 bits).
* The default value is 000000H.

24. High-bandwidth Digital Content Protection (HDCP)

24.1. Programmable Register Description

Address	Register Name	Attribute	Size
3CF, E3	HDCPCONFIG0	R/W	8-bit
3CF, E4	HDCPCONFIG1	R/W	8-bit
3CF, E5	HDCPI2CST	R/W	8-bit

3CF, E6	DBGADDR	R/W	8-bit
3CF, E7	DBGDOUT	R/W	8-bit
3CF, E8	DBGDATA	R/W	8-bit
3CF, ED-E9	BKSV	R/W	40-bit
3CF, EE	I2CADDR	R/W	8-bit
3CF, EF	I2CLEN	R/W	8-bit
3CF, F7-F0	AN	RO	64-bit
3CF, FC-F8	AKSV	RO	40-bit
3CF, FE-FD	AR0/ARI	RO	16-bit
3CF, FF	HSCPSTATUS	RO	8-bit

I2C

Address	Register Name	Attribute	Size	Default
3D5.37[7]	Read 1 for new chip whose SCL buffer is open collector	RO	1-bit	-
3D5.37[6]	1 st I2C SCL status	RO	1-bit	1
3D5.37[5]	Reserved	RO	1-bit	0
3D5.37[4]	2 nd I2C SCL signal(DVI/HDCP)	R/W	1-bit	1
3D5.37[3]	SDA operation: 0: Read; 1:Write	R/W	1-bit	0
3D5.37[2]	0: Enable 2 nd set; 1: Enable 1 st set	R/W	1-bit	0
3D5.37[1]	1 st I2C SCL signal (DDC/TV)	R/W	1-bit	1
3D5.37[0]	SDA signal	R/W	1-bit	0

24.2. HDCP Configuration 0

Address: 3CEH/3CFH Index: E3 Access: Read/Write

Bits 7:4 I2C SCL speed select. The default value is 00H.

Bits 3:0 Random AN select number. The default value is 0H.

24.3. HDCP Configuration 1

Address: 3CE/3CFH Index: E4 Access: Read/Write

Bit 7 Reserved.

Bit 6 Software reset. The default value is 0.

Bit 5 Enable counter 128 frame.
0: Disable (each frame) *
1: Enable

Bit 4 Reserved.

Bit 3 Reserved.

Bit 2 Reserved.

- Bit 1 Delay pipe adjustment for DE and SYNC.
0: 2 PCLK *
1: 1 PCLK
- Bit 0 Hot plug detect.
0: Not receiver connected *
1: Receiver connected

24.4. HDCP I2CST

Address: 3CE/3CFH Index: E5 Access: Read/Write

- Bit 7 Reserved.
- Bits 6:5 Reserved.
- Bit 4 Compare transmitter/receiver's R0/R1 is done or not.
0: Not ready yet *
1: Done
- Bit 3 Compare transmitter/receiver's R0/R1 is equal or not.
0: Not equal *
1: Equal
- Bit 2 Check receiver's revocation list is done or not.
0: Not yet *
1: Done
- Bit 1 Receiver's BKSv hit transmitter's revocation list.
0: Not hit *
1: Hit
- Bit 0 BKSv is ready for read or not.
0: Not ready yet *
1: Ready

24.5. HDCP BKSv

Address: 3CEH/3CFH Index: ED – E9 Access: Read/Write

- Bits 39:0 HDCP read back BKSv from receiver.
* The default value is 0000000000H.

24.6. HDCP I2C Address

Address: 3CEH/3CFH Index: EE Access: Read/Write

- Bit 7 I2C byte length bit 8. I2CLEN<7:0> is located at 3CF.EF.
* The default value is 0.
- Bits 6:0 I2C target address.
* The default value is 00H.

24.7. HDCP I2C Byte Length

Address: 3CEH/3CFH Index: EF Access: Read/Write

Bits 7:0 I2CLEN<7:0>.
* The default value is 00H.

24.8. HDCP Transmitter AN

Address: 3CEH/3CFH Index: F7 – F0 Access: Read Only

Bits 39:0 HDCP transmitter AN.
* The default value is 0000000000000000H.

24.9. HDCP Transmitter AKSV

Address: 3CEH/3CFH Index: FC – F8 Access: Read Only

Bits 39:0 HDCP transmitter AKSV.
* The default value is 0000000000H.

24.10. HDCP Transmitter AR0/AR1

Address: 3CEH/3CFH Index: FE - FD Access: Read Only

Bits 7:0 HDCP transmitter AR0/AR1.
* The default value is 0000H.

24.11. HDCP Status

Address: 3CEH/3CFH Index: FF Access: Read/Write

Bit 7 0: HDCP H/W I2C bus
1: S/W I2C bus *

Bits 6:3 Reserved.

Bit 2 HDCP AR0/AR1 is ready for read or not.
0: Not ready yet *
1: Ready

Bit 1 HDCP AKSV is ready for read or not.
0: Not ready yet *
1: Ready

25. Integrated TV-Out (TVX2) Controller Registers

The TVX2 has three major groups of registers that are described, in the following sections:

- Section 26.1 TV Encoder Control Registers
- Section 26.2 Macrovision 7.0x™ Control Registers
- Section 26.3 TV-Out Control and Filter Registers

The TV Encoder and Macrovision 7.0x™ Control registers are inter-related and occupy indexes from 00h to 3Fh. TV-Out Control and Filter registers occupy indexes from 80h to B7h.

24.1 TV Encoder Control Registers

Address Offset	Size	Name	Reset Value	Description
0x0, 0x1, 0x2, 0x3	32	CHROMA_FREQ	0x21F07C1F	Subcarrier/27,000,000*2^32
0x4	8	CHROMA_PHASE	0	Pre-set subcarrier phase control. Upper 8 bits (lower 24 bits are 0's).
0x5	8	RESERVED	0	Reserved for TV Encoder
0x6[7]	1	RGB_SETUP	0	Provides Black_level (0) or Blank_level (1) setup for RGB outputs.
0x6[6:4]	3	RGB_SYNC	0	Provides sync to RGB components: [2] =1 enables sync on R [1] =1 enables sync on G [0] =1 enables sync on B
0x6[3:1]	3	YC_DELAY	4	Relative pipeline delay between luma and chroma outputs (i.e. 0 = luma lags chroma by 4 clocks 4 = 0 clock 7 = chroma lags luma by 3 clocks).
0x6[0]	1	CVBS_ENABLE	1	Enables the composite and luma output.
0x7[3], 0x34[5]	2	CHROMA_BW	0	Chroma filter bandwidth control: 0=narrow 1=wide 2=extra wide 3=ultra wide.

Address Offset	Size	Name	Reset Value	Description
0x7[2]	1	COMP_YUV	0	Enables bypass on the RGB outputs to send component data YUV through.
0x7[1:0]	2	COMPCHGAIN	0	Percentage of chroma used in composite output: 00=100% 01=25% 10=50% 11=75%
0x8	8	HSYNC_WIDTH	126	Width of the Hsync in 27 MHz clks.
0x9[6:0]	7	BURST_WIDTH	68	Width of the burst in 27 MHz clks.
0xA	8	BACK_PORCH	118	Width of the back porch in 27 MHz clks.
0xB (signed)	8(s)	CB_BURST_LEVEL	59	C _b burst amplitude setting (-127 to 127)
0xC (signed)	8(s)	CR_BURST_LEVEL	0	C _r burst amplitude setting (-127 to 127).
0xD[1]	1	SLAVE_THRESH	0	Controls the threshold at which the encoder begins the horizontal line adjustments.
0xD[0]	1	SLAVE_MODE	0	Enables bit for encoder to operate under full slave-mode timing.
0xE, 0xF[1:0]	10	BLACK_LEVEL	282	Used to create a setup.
0x10, 0x11[1:0]	10	BLANK_LEVEL	240	Blanking level during non-VBI.
0x17, 0x18[1:0]	10	NUM_LINES	525	Number of lines in a frame. (Odd implies an interlace image, even implies a progressive image).
0x1E, 0x1F[1:0]	10	WHITE_LEVEL	800	White level.
0x20	8	CB_GAIN	137	C _b color saturation control (1LSB=1/128).
0x22	8	CR_GAIN	137	C _r color saturation control (1LSB=1/128).
0x25	8	TINT	0	Tint adjustment on chroma.
0x29[4:0]	5	BREEZE_WAY	22	Width of the breezeway in 27 MHz clks.
0x2C[5:0]	6	FRONT_PORCH	32	Width of the front porch in 27 MHz clks.
0x31, 0x32[2:0]	11	ACTIVELINE	1440	Number of 27 MHz clks in active video line.
0x33	8	FIRST_VIDEOLINE	21	Line number for first line of video in field.
0x34[7]	1	UV_ORDER	0	1 = switches the ordering of C _b and C _r inputs.

Address Offset	Size	Name	Reset Value	Description
0x34[6]	1	PAL_MODE	0	0 = NTSC format
0x34[4]	1	INVERT_TOP	0	Invert the polarity of TV encoder's field identification signal.
0x34[3]	1	SYS625_50	0	0 = 525 lines 59.94 fields/s system 1 = 625 lines 50 fields/s system
0x34[0]	1	VSYNC5	0	0 for six equalization and broad pulses.
0x34[2:1]	2	CPHASE_RST	1	Resetting period of carrier block 0 = every 8 fields 1 = every 4 fields 2 = every other line 3 = once before any chroma bursts.
0x35	8	SYNC_LEVEL	72	Sync level during blanking periods.
0x3C, 0x3D[1:0]	10	VBI_BLANK_LEVEL	296	Blanking level during non-VBI.
0x3E[0]	1	SOFT_RESET	1	0 = starts TV timing generation
0x3F	8	PRODUCT_VERSION	0x10	Read-only product version number

24.2 Macrovision™ 7.0x Control Registers

Address Offset	Size	Name	Reset Value	Description
0x12[5:0]	6	N1	0x17	Colorstripe definition # 1.
0x13[5:0]	6	N3	0x21	Colorstripe definition # 3.
0x14[5:0]	6	N8	0x1B	Pseudo-sync pulse parameters # 1.
0x15[5:0]	6	N9	0x1B	Pseudo-sync pulse parameters # 2.
0x16[5:0]	6	N10	0x24	Pseudo-sync pulse parameters # 3.
0x19	8	N0	0x3E	On/off and mode control.
0x1A	8	N13	0x0F	Individual pseudo-sync/AGC pulse on/off, format A.
0x1B	8	N14	0x0F	Individual pseudo-sync/AGC pulse on/off, format B.
0x1C	8	N15	0x60	End of field back porch pulse configuration.
0x1D[2:0]	3	N5	0x5	Colorstripe definition # 5

Address Offset	Size	Name	Reset Value	Description
0x21[2:0]	3	N20	0x4	Subcarrier phase: zone 1.
0x23[0]	1	N16	0x1	Burst advanced start on/off.
0x24[3:0]	4	N7	0x2	Colorstripe definition # 7.
0x26[3:0]	4	N17	0xA	Start of burst to 1 st phase switch point duration.
0x27[3:0]	4	N19	0x5	2 nd phase switch point to end of burst.
0x28[3:0]	4	N18	0x0F	1 st to 2 nd phase switch point duration.
0x2A, 0x2B[1:0]	10	N21	0x3FF	Colorstripe 1 st line phase.
0x2D, 0x2E[6:0]	15	N11	0x07F8	Pseudo-sync/AGC pulses: line numbers select.
0x2F, 0x30[6:0]	15	N12	0x0000	Pseudo-sync/AGC pulses: A/B format selection by line number.
0x36[0]	1	N22	0x0	RGB definition.
0x39[6:0]	7	N4	0x15	Colorstripe definition # 4.
0x3A[2:0]	3	N6	0x5	Colorstripe definition # 6.
0x3B[6:0]	7	N2	0x15	Colorstripe definition # 2.
0x37	8	AGC_PULSE_LEVEL	163	Amplitude of MV pseudo-sync AGC pulses, upper 8-bit out of 10-bit.
0x38	8	BP_PULSE_LEVEL	200	Back porch pulse level, upper 8-bit out of 10-bit.

24.3 TV Out Control and Filter Registers

24.3.1 Input Data Format Control Registers

Address Offset	Size	Name	Reset Value	Description
0x9E[5]	1	CSCPASS	0	Bypass color space converter. 0 = RGB data input format, and 1 = CCIR data input format.
0x9E[4]	1	UVINV	0	C _b /C _r components of TV Out swapping. 0 = C _b after C _r in Chroma data, and 1 = C _b before C _r in Chroma data. <i>Set UVINV = 1 unless specified otherwise.</i>

Address Offset	Size	Name	Reset Value	Description
0xA2[5]	1	INSWAP1	0	Swapping input data MS 8-bit with LS 8-bit (only work with 8-bit multiplexed data mode). 1 = 8-bit Multiplexed CCIR format as in section 2.2.1, YUV422 (C _b YC _r Y) mode 0 = Other Input Formats.
0xA2[4]	1	INSWAP2	0	Swapping input data MS 8-bit with LS 8-bit. Internal Data Format Control. <i>Set INSWAP2 = 0 unless specified otherwise.</i>
0xAD[3]	1	REG_RGB24	0	Select input format YUV/RGB, 1 enables RGB24 format. 1 = 12-bit Multiplexed RGB24 mode as in section 2.2.2 0 = Other Input Data Formats.

24.3.2 Horizontal Processing Unit Control Registers

Address Offset	Bits	Name	Reset Value	Description
0xA9[7]	1	REG_Y_FILT_EN	0	<i>Y low-pass filter enable</i> <i>1 = Low-Pass Filter enable</i> <i>0 = bypasses Low-Pass Filter</i>
0xA9[6]	1	REG_UV_FILT_EN	0	UV low-pass filter enable 1 = Low-Pass Filter Function 0 = Bypass Low-Pass Filter Function.
0xA9[5]	1	REG_UV_SIGN		UV Sign Enable 1 = UV or C _b C _r data as signed data. 0 = Unsigned data.
0xA9[4]	1	REG_CUBEEN	0	Bilinear Enable 1 = Bi-linear Scaling Function is enabled. 0 = Bypasses Bi-linear Scaling Function.

0xA9[3:0]	4	REG_GAIN	0	<i>Gain value in Sharp filter.</i> <i>This register helps decide the level of sharpness to be achieved.</i>
0xAA[7:0], 0xAC[5:4]	10	REG_HCF_R	0	Scaling Factor Control Scaling down ratio multiplied by 1024; i.e., (Destination / Source) x 1024, where only integers are considered and fractions are ignored. Where, Source: Size of the Source Picture; Destination: Size of the Picture after scaling.
0xAB[7:0], 0xAC[3:2]	10	REG_HCF_1	0	Scaling Factor Control. Inverter of REG_HCF_R; i.e., = (Source / Destination), format as XXXX_*****, where the first 4 bits are integers and the next 6 bits are fractions. Where, Source: Size of the Source Picture; Destination: Size of the Picture after scaling.
0xAC[6]	1	REG_SIGN_UV_MUX	0	Sign control bit for UV_MUX module in horizontal processing. If =0; bypass input data; If = 1; invert msb of input data
0xAC[1]	1	REG_SHARP_EN	0	Sharp filter enable 1 = Sharpness Function enable 0 = Sharpness Function bypassed.
0xAC[0]	1	REG_SEL	0	1 = 5-pixel sharpness function 0 = 3-pixel sharpness function

24.3.3 Scan Conversion And Vertical Filtering Control Registers

Address Offset	Size	Name	Reset Value	Description
0x82[3:0], 0x81	12	MF	N/A	Dropline parameter.
0x83[7]	1	REG_LUMA_ADD16	0	Add 16 to Y if = 1; bypass if = 0

Address Offset	Size	Name	Reset Value	Description
0x82[3:0], 0x81	12	MF	N/A	Dropline parameter.
0x83[6]	1	REG_CHROMA_SIG N	0	Invert sign bit of chroma if = 1; bypass if = 0
0x83[5:4]	2	REG_MODE4C[1:0]	0	Vertical chroma filter mode select: See Table 3.3.3.2
0x83[3:1]	3	REG_MODE4Y[2 :0]	0	Vertical luma filter mode select: See Table 3.3.3.1

24.3.4 Luma Fitter Table

NAME: REG_MODE4Y[2:0]	ADDRESS: 0x83[3:1]	<i>Filter Mode</i>
Settings:	000	Bypass Filter, no effects
	010	3 Tap, low filtered effects
	011	3 Tap, high filtered effects
	100	4 Tap, low filtered effects
	101	4 Tap, high filtered effects
	Others	Reserved

24.3.5 Chroma Fitter Table

NAME: REG_MODE4C[1:0]	ADDRESS: 0x83[5:4]	Filter Mode
<i>Settings:</i>	00	Bypass Filter, no effects
	10	3 Tap, low filtered effects
	11	3 Tap, high filtered effects
	01	Reserved

24.3.6 TV CRTC Control Registers

Address Offset	Size	Name	Reset Value	Description
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0x86	8	T_HSWIDTH	N/A	TV CRTC Hsync width, # is in pixels.
0x87[7:4]	4	T_VSWIDTH	N/A	TV CRTC Vsync width, # is in lines.
0x89[4:0], 0x88	13	T_HSTART	N/A	TV CRTC horizontal data start number, in pixels.
0x8D[5:0], 0x8C	14	T_HEND	N/A	TV CRTC horizontal data end number, in pixels.
0x8B[5:0], 0x8A	14	T_HTOTAL	N/A	TV CRTC horizontal total pixels.
0x8F[7:4], 0x8E	12	T_VSTART	N/A	TV CRTC vertical start line number.
0x8F[3:0], 0x90	12	T_VEND	N/A	TV CRTC vertical end line number.
0x87[3:0], 0x91	12	T_VTOTAL	N/A	TV CRTC vertical total lines.
0x89[7]	1	TCLKBY2	1	Enables TV double clks.
0x89[6]	1	T_FRSTEN	1	Enables TV CRTC frame reset, slave =1.
0x89[5]	1	T_INTERLACE	1	Enables TV CRTC interlace mode.
0x8B[7]	1	T_HRSTEN	0	Enables TV CRTC horizontal reset by external Hsync.
0x8B[6]	1	T_VRSTEN	1	Enables TV CRTC vertical reset by external Vsync.
0x8D[7]	1	T_HLOADEN	1	TV CRTC horizontal load enable.
0x8D[6]	1	T_VLOADEN	1	TV CRTC vertical load enable.
0xA2[1]	1	VRSTC	0	TV CRTC Vertical reset control.
0xA2[0]	1	FIELDINV	0	Swapping the field output of TV CRTC.

Definition of Terms:

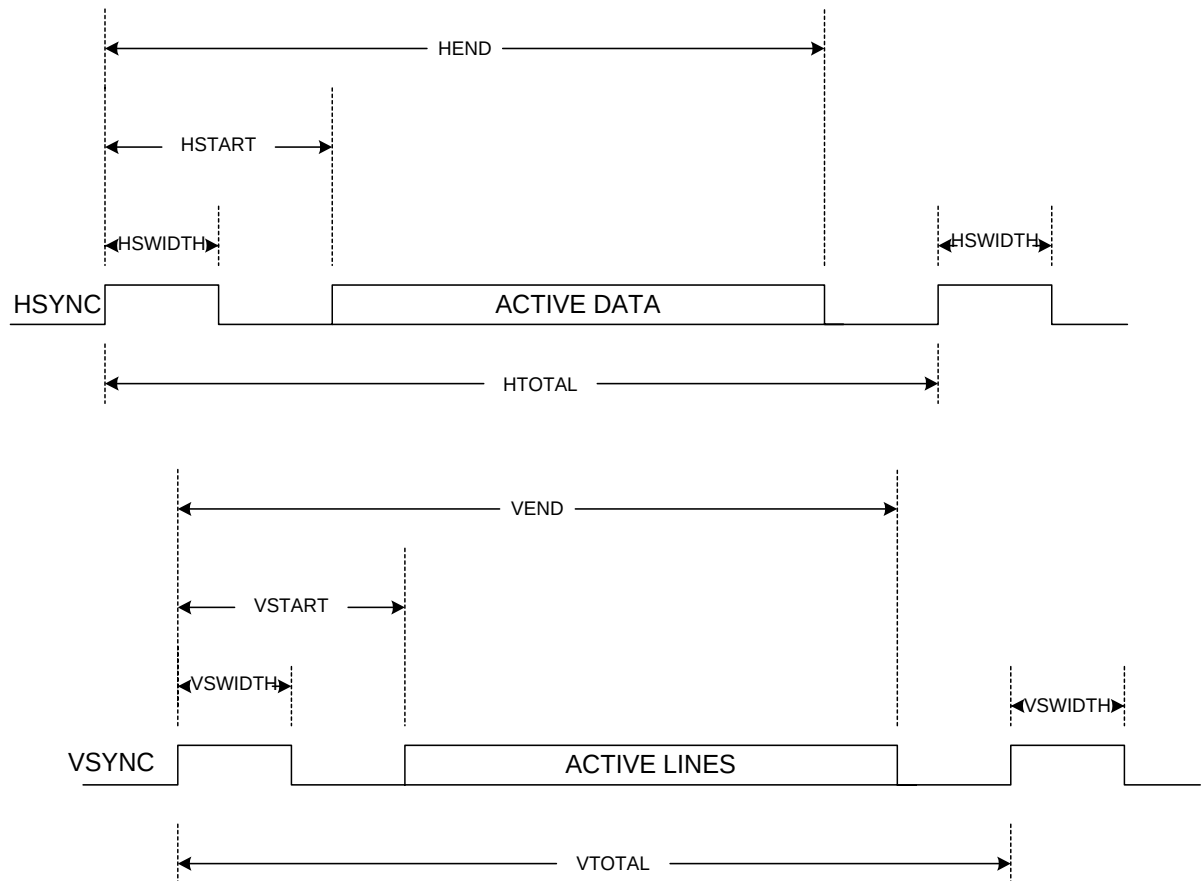


Figure 26.1 Definition of Terms

24.3.7 VGA CRTC Control Registers

Address Offset	Size	Name	Reset Value	Description
0x92	8	V_HSWIDTH	N/A	VGA CRTC Hsync width, # is in pixels.
0x93[7:4]	4	V_VSWIDTH	N/A	VGA CRTC Vsync width, # is in pixels.
0x95[4:0], 0x94	13	V_HSTART	N/A	VGA CRTC horizontal data start number, in pixels.
0x99[5:0], 0x98	14	V_HEND	N/A	VGA CRTC horizontal data end number, in pixels.
0x97[5:0], 0x96	14	V_HTOTAL	N/A	VGA CRTC horizontal total pixels.
0x9B[7:4], 0x9A	12	V_VSTART	N/A	VGA CRTC vertical start line number.
0x9B[3:0], 0x9C	12	V_VEND	N/A	VGA CRTC vertical end line number.
0x93[3:0], 0x9D	12	V_VTOTAL	N/A	VGA CRTC vertical total lines.

Address Offset	Size	Name	Reset Value	Description
0x95[7]	1	VCLKBY2	0	Enables VGA double clks.
0x95[6]	1	V_FRSTEN	0	Enables VGA CRTC frame reset.
0x95[5]	1	V_INTERLACE	0	Enables VGA CRTC interlace mode.
0x97[7]	1	V_HRSTEN	0	Enables VGA CRTC horizontal reset by external Hsync.
0x97[6]	1	V_VRSTEN	1	Enables VGA CRTC vertical reset by external Vsync.
0x99[7]	1	V_HLOADEN	1	VGA CRTC horizontal load enable.
0x99[6]	1	V_VLOADEN	1	VGA CRTC vertical load enable.
0x9E[7]	1	EXTHVSEL	1	0=chip input HVsync 1=chip input HVDE
0x9E[6]	1	EXTHVINV	1	Enables swapping external H/V sync signals.

Definition of Terms: See Figure 26.1.

24.3.8 TV PLL Control Registers

Address Offset	Size	Name	Reset Value	Description
0xA4, 0xA3	16	IVD	96AD	Register control for TCLK.
0xA6[6]	1	REG_PLL_SET_EN	0	PLL uses register settings if =1; PLL uses default constant settings if = 0
0xA6[5]	1	REG_EN_SET	0	0 to 1 transition load REG_PATTERN for PLL
0xA6[4]	1	REG_N_SELECT	0	Old N value for PLL if = 0; new if = 1
0xB1, B0, AF, AE	32	REG_PATTERN[31:0]	0	Reserved for PLL settings

After System Reset, TV PLL takes the IVD[15:0] default value and generates a 27 MHz TV clock for TVX2.

To change the TV PLL setting to new values, do the following:

1. Set REG_PLL_SET_EN = 0, REG_N_SELECT = 0 as TV PLL will use the default values.
2. Set IVD[15:0] to new values that are desired.
3. Set REG_PLL_SET_EN = 1, so that the new values are enabled.

A Fractional-Synthesizer is implemented to improve the precision of the TV PLL frequency. To enable the Fractional-Synthesizer, do the following:

1. Set REG_PLL_SET_EN = 0.
2. Set IVD[15:0] to values that are desired.
3. Load REG_PATTERN[31:0] with desired values.
4. Toggle REG_EN_SET in the 0 → 1 → 0 sequence.
5. Set REG_N_SELECT = 1 to enable the fractional-synthesizer.
6. Set REG_PLL_SET_EN = 1 to transfer the new settings to TV PLL.

24.3.9 Clock and Power Management Registers

Address Offset	Size	Name	Reset Value	Description
0x9E[0]	1	SLEEPALL	0	Enables entire chip sleep mode.
0x9F[1]	1	XCLKBY2	0	Enables external XCLK double clk output.
0x9F[0]	1	CLKINV	0	Enables inverter of double clk of XCLK.
0xA0[7:4]	4	SLEEP	0	DAC sleep control.
0xA2[3]	1	SUSPEND	0	Chip suspend.
0xA5[4:3]	2	UNICLK	0	Enables TV CLK directly connecting to XCLK.
0xA5[2]	1	XCLKOFF	0	Turn off the external CLK
0xA5[1]	1	TCLKOFF	0	Internal TV CLK turn off
0xA5[0]	1	OSCDIS	0	TCLK PLL Osc. disable
0xA6[7]	1	XCLKD	0	Reserved
0xA7[7:4]	4	REG_RISE_CTRL[3:0]	0	Delay VCLK rising edge by 0-15 ns
0xA7[3:0]	4	REG_FALL_CTRL[3:0]	0	Delay VCLK falling edge by 0-15 ns

24.3.10 Sync Line Buffer Control Registers

Address Offset	Size	Name	Reset Value	Description
0xAD[5]	1	REG_LB_RST	0	Program to generate a high active pulse to reset sync

Address Offset	Size	Name	Reset Value	Description
				line buffer read/write function
0xAD[4]	1	REG_LB_STATUS	0	When 1, enable host access sync line buffer
0xAD[3]	1	REG_RGB24	0	Select input format YUV/RGB, 1 enables RGB format
0xAD[2]	1	REG_REFRESH	0	Enables sync line buffer to be filled by sync module
0xAD[1]	1	ENVGAVS	0	Enables VGA VS for sync module stimulation
0xAD[0]	1	REG_MODE_SELECT	0	1: Enables sync line buffer control VGA to TV line translate, 0: Don't use sync line buffer
0xB3	8	WRITE SYNC BUF	N/A	Host write to sync line buffer
0xB4	8	READ SYNC BUF1	Read only	Host read from sync line buffer
0xB5	8	READ SYNC BUF2	Read only	Host read from sync line buffer

Enabling the Sync Line Buffer

The following are the procedures to enable the Sync Line Buffer:

1. Always set AD[1] = 1;
2. When AD[2] = 1; the bit enables the sync line buffer to be filled automatically. Wait for at least two fields (>33.3 ms for NTSC, > 40 ms for PAL).
3. When AD[2] = 0; the bit stops filling the sync line buffer.
4. When AD[0] = 1; the bit enables the sync line buffer control to be used.

Reading/Writing to the Sync line buffer from the Host

The following are the procedures to read / write to the Sync Line Buffer from the Host:

1. Always set AD[1] = 1;
2. When AD[4] = 1; the bit enables the host to access the Sync Line Buffer.
3. When AD[5] = 1; the bit generates a reset pulse.
4. AD[5] = 0;

B3 should be used to write to the Sync line Buffer. B4 and B5 should be used to read from the Sync Line Buffer, in the following sequence: B3, B4, B3, B4, B3, B4...

Disabling the Sync Line Buffer

The following are the procedures to disable the Sync Line Buffer:

Set AD[5:0] = 0; This is the default value.

24.3.11 Miscellaneous Registers

Address Offset	Size	Name	Reset Value	Description
0x80	8	TVX_VERSION_ID	0	TVX2 product version (read only).
0x82[7:4]	4	NO-USE	N/A	
0x83[0]	1	SYN_W3E_SELECT	0	If = 1, use sync'd W3E; else use old W3E
0x84[7:0]	8	NO-USE	N/A	
0x85[7:0]	8	NO-USE	N/A	
0x9E[3]	1	EN_TESTDAC	0	Enables DAC test through pin input data; if = 1, test data goes to DAC; if = 0, SSDATA from register 0xA2 and 0xA1 goes to DAC.
0x9E[2]	1	TVBLUE	0	Enables full screen blue pattern.
0x9E[1]	1	SCANEN	0	Enables scan insertion test mode
0x9F[7]	1	FINISH1	0	Software start.
0x9F[6]	1	TVOUTPASS	0	Bypass TV Out block.
0x9F[5]	1	TESTEN	0	Enables chip test mode
0x9F[4:2]	3	TESTDATSEL	0	9-bit test data output selection: 0=DACin1; 1=DACin2; 2=DACin3; 3=TvoutL; 4=TvoutH; 5,6,7=mixed signal.
0xA2[6]	1	DATINSEL	0	0 = 8-bit multiplexed data 1 = 16-bit demultiplexed data input
0xA0[2]	1	SVIDEO	1	S-Video output enable.
0xA0[1]	1	SCART	0	SCART output enable.
0xA0[0]	1	CVBS	1	CVBS output enable.
0xA0[3]	1	SSPULSE	0	DAC sensor sleeping pulse.
0xA2[7], 0xA1	9	SSDATA	0	DAC sensor sleeping data.
0xA2[2]	1	MASTEREN	0	Chip master mode enable.
0xA5[7:5]	3	MASTERP	0	Individually control the H, V, XCLK output enable.

Address Offset	Size	Name	Reset Value	Description
0xA6[3]	1	RESERVED	0	0 = PLL output (TCLK) to port TVTESTO[7] for PLL test pattern. 1 = Function test, data output to port TVTESTO[7].
0xA6[2:0]	3	BIST_ON	0	Enables video line buffer BIST test mode.
0xA8[7]	1	VBLANK	N/A	CVE2 vertical blank signal (read only)
0xA8[6]	1	CVE_FIELD	N/A	CVE2 field output (read only)
0xA8[5]	1	RCOMP_Y	N/A	Luma out sensor (read only).
0xA8[4]	1	RCOMP_C	N/A	Chroma out sensor (read only).
0xA8[3]	1	RCOMP_CVBS	N/A	Composite out sensor (read only).
0xA8[2:1]	2	BIST_ERROR	N/A	BIST error report (read only).
0xA8[0]	1	BIST_ERROR	N/A	OR'd BIST error of all line buffers in vfilter (read only).
0xAC[7]	1	REG_OVS_SEL	0	Select output Vsync Signal: =1, the output Vsync signal is sync'd with input VGA Hsync; = 0, not sync'd.
0xAD[7:6]	2	REG_MATCH_VHDE_C[1:0]	0	Control VHDE pipeline match-up in different mode: 00 for no horizontal scaling mode; 01 for 8x6 to NTSC; 10 for TBD; 11 for TBD
0xB2[7:6]	2	RESERVED	N/A	Reserved.
0xB2[5]	1	RESERVED	0	Reserved (Default is 0).
0xB2[4]	1	RESERVED	0	Reserved (Default is 0).
0xB2[3]	1	REG_SWAP_INVERT	0	Swap U/V of self test signal.
0xB2[2]	1	REG_PAL_EBU_BAR	0	1 = PAL 0 = NTSC
0xB2[1]	1	REG_Y_RAMP	0	1 = Ramp 0 = Color Bar
0xB2[0]	1	Self_test_en	0	1 = self test 0 = normal working mode
0xB6[5:0]	6	RESERVED	N/A	BIST error 6 to 1 of line buffers in vfilter (read only).
0xB8[7]	1	LOAD_PARAMETER_EN	0	1 = Load register for vfilters

Address Offset	Size	Name	Reset Value	Description
0xB8[6:0]	7	WY_A	0	Yfilter parameter.
0xB9[7]	1	ODD_EVEN_B	0	0 = Even 1 = Odd
0xB9[6:0]	7	WY_B	0	Yfilter parameter.
0xBA[7]	1	BY_PASS	0	0 = No change 1 = Bypass vfilter
0xBA[6:0]	7	WY_C	0	Yfilter parameter.
0xBB[7]	1	EN_V_2PIN	0	0 = Function test data to monitor pin TVTESTO[0] 1 = Vsync output to monitor pin TVTESTO[0]
0xBB[6:0]	7	WY_D	0	Yfilter parameter.
0xBC[7]	1	RESERVED	0	
0xBC[6:0]	7	WC_A	0	Cfilter parameter.
0xBD[7]	1	ODD_EVEN_B	0	0 = Even 1 = Odd
0xBD[6:0]	7	WC_B	0	Cfilter parameter.
0xBE[7]	1	BY_PASS	0	0 = No change 1 = Bypass vfilter
0xBE[6:0]	7	WC_C	0	Cfilter parameter.
0xBF[7]	1	RESERVED	0	
0xBF[6:0]	7	WC_D	0	Cfilter parameter.